Application Note

SL1680 General PCB Design and LPDDR4 & LPDDR4(x) Interface Layout Guidelines

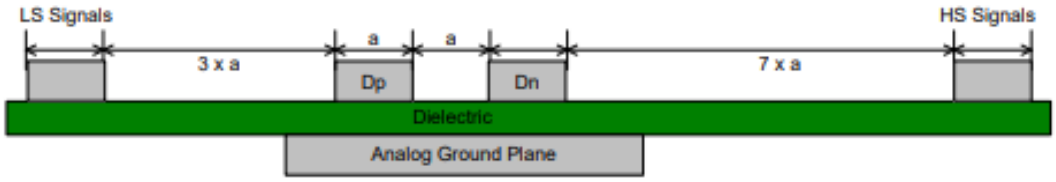
Abstract: This document provides PCB design and layout guidelines for integrating the Synaptics SL1680 with LPDDR4 and LPDDR4x memory, detailing routing rules, power supply considerations, impedance requirements, and best practices to ensure optimal signal integrity and performance.

  | PN: 506-001390-01 Rev E

Contents

1. PCB Layout Guidelines

- Trace impedance of 100ohm differential (+/-10%) is required. For USB2.0, the trace impedance of 90ohm differential (+/-10%) is required.
- Matching to < 0.5mm (about 0.02 inch) between two different signals. Trace lengths should match by 0.25mm (about 0.01 inch) or less for differential pairs (same pair) of high-speed signals.
- The skew between any data lane and clock lane should be matched within +/-10ps on both package and PCB.
- Do not route trace over plane void or anti-pads. Return path should be VSS and continuous.
- Ensure ground return vias adjacent to the differential pair core vias to minimize crosstalk between lanes.
- Void the planes above the BGA pads to minimize the capacitive discontinuity.
- To minimize crosstalk, take care of signal traces which are routed close to the data differential pairs. The minimum recommended spacing is 3xa for low-speed non-periodic signals and 7xa for high-speed periodic signals. A continuous ground plane below the differential lines is required.



- TX and RX pairs should not be routed side-by-side in the same signal layer.
- Crosstalk should be accumulated total with all aggressors and meet the
- -30dB requirement until Nyquist frequency.
- The insertion loss of the trace is < 3dB (at Nyquist). For PCIE3.0, USB3.0 and Ethernet, the insertion loss of trace can be < 6dB. It should be monotonic, with no large insertion loss variations (+/-2dB) in the Nyquist frequency range. Trace should be shortest and low-loss as possible.

2. Power Supply Guidelines

- Supply bypass capacitors are recommended to minimize power supply noise. Noise analysis of the power delivery network is required to determine the actual values. Depending on their size, each capacitor will have a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that will determine the given capacitor's effectiveness over a frequency range. In general, several low-value capacitors (ceramic-type capacitors) should be placed as close as possible to the package pins. Larger-value capacitors (tantalum/electrolytic-type capacitors) can be placed farther away.
- The supply bypass capacitors should be connected as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane / trace as possible to reduce inductive and resistive losses. Typical capacitor placement can be under the package (other side of the board) or on the same side but close. An example of bypass capacitors is shown below.

Component	Value[1]
Power Supply Bypass Capacitors	0.01 µF, 0.1 µF, 4.7 µF, 10.0 µF

1. Smaller-value capacitors must be placed between the ferrite bead and the package.

- Both power plane and ground plane should be maintained continuously and have solid return path (not in bits and pieces). Pay attention to the void areas caused by vias. If the planes are cut down by vias, we need to compensate for the loss of the plane shape to make sure the effective width of the plane.

3. 4L non-HDI PCB Design Rules

3.1. NSMD Pad

- Minimum pin pitch = 0.4 mm (15.75 mil)
- Footprint pad / Paste mask of pad = 10mil (bga10)
- Solder mask of pad = 10 mil

3.2. SMD Pad

- Minimum pin pitch = 0.381 mm (15 mil)
- Footprint pad / Paste mask of pad = 12 mil (bga12)
- Solder mask of pad = 8 mil

3.3. Via

- Minimum through hole pad / Drill size = 14 / 8 mil

3.4. Spacing

- Minimum trace-to-trace = 3 mil
- Minimum trace-to-via = 3 mil
- Minimum trace-to-pad = 3 mil

The example stack-up/trace width and spacing of 4L non-HDI PCB is shown below.

Stack-up		Thickness(mil)			DK	Df	Material
	SM_TOP (0.5_PT_1OZ)	0.5			3.4		
L1			1.654	0.333oz +Plating			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L2			1.26	1oz			
	Core+PP (1.3mm)	51.18			4.6	0.018	S1000-2M
L3			1.26	1oz			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L4			1.654	0.333oz +Plating			
	SM_BOT (0.5_PT_1OZ)	0.5			3.4		
Thickness(mil):	63.988	63.988					
FinishPCBThinckness(mm):	1.6 (+/-0.16) mm						
PressPCBThinkness(mm):	1.48 (+/-0.08) mm						

Number	Type	Control Layer	Referance Layer	Adjust Line Width (mil)	Adjust Spacing (mil)	Adjust Line To Copper (mil)	Design Impedance (ohm)
1	Single-End	L1/L4	L2/L3	3.6			55.01
2	Single-End	L1/L4	L2/L3	4			52.93
3	Single-End	L1/L4	L2/L3	4.5			50.15
4	Differential	L1/L4	L2/L3	3.5	3		84.62
5	Differential	L1/L4	L2/L3	3.6	4		90.11
6	Differential	L1/L4	L2/L3	3.4	5.8		99.3
7	Differential	L1/L4	L2/L3	4	4		88.41

4. PCB Routing Rules for SL1680 LPDDR4/LPDDR4x Interface

Notes:

- This guideline recommends optimal layout practices for the DRAM section and is not a set of strict limitations.
- Synaptics reference layouts follow the guidelines, ensuring good operating timing margins.

4.1. General Rules

The general rules of usage are:

- All signals must be routed with a solid reference layer.
- Route single-end DQ[x] on the same layer within each BYTE group. If different layers are used, account for varying propagation delays during electrical length matching.
- Bit order can be scrambled within the same byte group for easier routing.
- The impedance of single-ended signals should be 50 ohms +/- 10%. (It may be 55 ohms +/- 10% in the BGA break-out area).
- The impedance of differential pairs should be 85 ohms +/- 10%.
- Include via delay in length matching calculations.
- Place 1nF/10nF capacitors near each power pin of the SoC and all DRAMs for effective decoupling.
- Place 1nF/10nF capacitors at the edge of the power plane to reduce resonance.
- Place 1uF/10uF capacitors at the power rail input for both SoC and DRAM to avoid power trace bottlenecking.
- Place ground vias as close as possible to the cluster of signals vias.
- No more than two vias are recommended on any signal between the SoC and DRAMs, excluding low-speed DDR RSTn.

4.2. Package Trace Length Compensation

The following are considerations for compensation:

- Trace lengths between chip die and package pins were not matched well due to package geometry, resulting in different propagation delays for each signal on the package substrate. These differences will impact timing margin. To compensate for this mismatch, proper PCB routing is essential. Refer to the table below for the electrical length of individual traces.
- Note that the compensation should be made in addition to any special trace matching or tuning requirements mentioned in the sections that follow.
- The detailed constraint information can be found in the Synaptics reference layout files.

North Side

ADDRESS / COMMAND / CONTROL Group			Byte Lane 0 Group			Byte Lane 1 Group		
Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)
J31	M0_CKP	25.50	B42	M0_DM[0]	44.52	C32	M0_DM[1]	31.99
L31	M0_CKN	22.91	E39	M0_DQ[0]	36.61	C34	M0_DQ[8]	35.85
G31	M0_A[0]	29.15	G39	M0_DQ[1]	31.54	G35	M0_DQ[9]	32.42
N31	M0_A[1]	19.25	C40	M0_DQ[2]	36.41	B30	M0_DQ[10]	35.97
C27	M0_A[2]	30.88	C38	M0_DQ[3]	33.75	C30	M0_DQ[11]	31.59
C26	M0_A[3]	28.97	N39	M0_DQ[4]	26.02	B35	M0_DQ[12]	41.39
G27	M0_A[4]	24.24	A42	M0_DQ[5]	49.31	C36	M0_DQ[13]	36.53
E27	M0_A[5]	25.15	C43	M0_DQ[6]	42.97	A35	M0_DQ[14]	40.36
A28	M0_CKE	39.25	B43	M0_DQ[7]	43.77	B36	M0_DQ[15]	36.14
B28	M0_CSN	38.56	J39	M0_DQSP[0]	30.82	J35	M0_DQSP[1]	27.64
			L39	M0_DQSN[0]	29.63	L35	M0_DQSN[1]	26.43

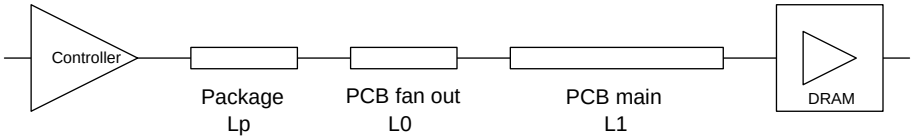
ADDRESS / COMMAND / CONTROL Group			Byte Lane 2 Group			Byte Lane 3 Group		
Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)
L23	M1_CKP	22.06	E15	M1_DM[0]	27.23	B4	M1_DM[1]	37.57
J23	M1_CKN	20.80	C11	M1_DQ[0]	35.66	A3	M1_DQ[8]	44.76
B22	M1_A[0]	33.51	C14	M1_DQ[1]	33.54	C6	M1_DQ[9]	35.94
G23	M1_A[1]	22.25	C12	M1_DQ[2]	31.63	B3	M1_DQ[10]	39.53
C19	M1_A[2]	31.89	B11	M1_DQ[3]	33.03	C4	M1_DQ[11]	34.35
G19	M1_A[3]	23.93	B16	M1_DQ[4]	37.67	G11	M1_DQ[12]	29.36
A22	M1_A[4]	38.10	A16	M1_DQ[5]	38.72	C8	M1_DQ[13]	35.35
C20	M1_A[5]	30.65	C18	M1_DQ[6]	30.30	A10	M1_DQ[14]	38.38
C24	M1_CKE	34.36	B18	M1_DQ[7]	30.92	B10	M1_DQ[15]	33.68
B24	M1_CSN	31.28	L19	M1_DQSP[0]	21.51	J15	M1_DQSP[1]	22.01
			J19	M1_DQSN[0]	20.55	L15	M1_DQSN[1]	20.61

West Side

ADDRESS / COMMAND / CONTROL Group			Byte Lane 0 Group			Byte Lane 1 Group		
Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)
AC11	M2_CKP	20.35	D2	M2_DM[0]	44.38	P3	M2_DM[1]	32.69
AC9	M2_CKN	21.27	C2	M2_DQ[0]	47.67	L7	M2_DQ[8]	38.12
AC13	M2_A[0]	13.71	D3	M2_DQ[1]	38.47	R5	M2_DQ[9]	29.49
AB2	M2_A[1]	35.51	F3	M2_DQ[2]	38.23	L3	M2_DQ[10]	34.61
AC7	M2_A[2]	22.73	C1	M2_DQ[3]	48.88	R7	M2_DQ[11]	25.36
W3	M2_A[3]	28.58	H3	M2_DQ[4]	41.44	W7	M2_DQ[12]	25.10
AB1	M2_A[4]	34.18	K2	M2_DQ[5]	40.11	T1	M2_DQ[13]	34.48
Y3	M2_A[5]	29.18	K1	M2_DQ[6]	38.29	M3	M2_DQ[14]	36.78
V3	M2_CKE	31.17	L2	M2_DQ[7]	33.26	T2	M2_DQ[15]	34.91
V2	M2_CSN	38.68	R11	M2_DQSP[0]	27.30	W11	M2_DQSP[1]	21.83
			R9	M2_DQSN[0]	22.54	W9	M2_DQSN[1]	20.86

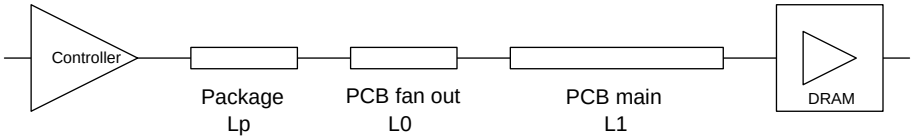
ADDRESS / COMMAND / CONTROL Group			Byte Lane 2 Group			Byte Lane 3 Group		
Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)	Pin	Signal	Package Propagation Delay (ps)
AL11	M3_CKP	14.52	AP3	M3_DM[0]	26.63	BB1	M3_DM[1]	33.03
AL9	M3_CKN	17.28	AK3	M3_DQ[0]	28.32	AY3	M3_DQ[8]	31.47
AF3	M3_A[0]	25.53	AK2	M3_DQ[1]	28.30	AW5	M3_DQ[9]	28.48
AG7	M3_A[1]	20.63	AM3	M3_DQ[2]	28.60	AV3	M3_DQ[10]	25.96
AG5	M3_A[2]	26.51	AH2	M3_DQ[3]	28.37	AT3	M3_DQ[11]	24.18
AG3	M3_A[3]	30.07	AR7	M3_DQ[4]	22.19	AW7	M3_DQ[12]	26.45
AL7	M3_A[4]	21.37	AR2	M3_DQ[5]	26.11	BC3	M3_DQ[13]	31.77
AH1	M3_A[5]	32.60	AT2	M3_DQ[6]	27.49	BB2	M3_DQ[14]	29.91
AD2	M3_CKE	35.88	AR1	M3_DQ[7]	32.14	BC2	M3_DQ[15]	31.21
AD3	M3_CSN	28.44	AR11	M3_DQSP[0]	18.70	AW9	M3_DQSP[1]	20.78
			AR9	M3_DQSN[0]	18.01	AW11	M3_DQSN[1]	18.86

4.3. Data (DQ/DQM/DQS) Bus



- All signals use point-to-point routing topology.
- DQS must be routed in pairs on the same layer to match the propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- The total trace length (L0 + L1) is recommended to be no longer than 1200 mils to minimize attenuation.
- For each byte lane, the length matching for DQ(DM) to DQ(DM (Lp + L0 + L1)) should be within +/-5ps.
- For each byte lane, the length matching for DQS to DQ(DM) (Lp + L0 + L1) should be within +/-10ps.
- For each byte lane, the length matching for DQSp to DQSn (Lp + L0 + L1) should be within +/-0.5ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between differential (DQSp / DQSn) to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

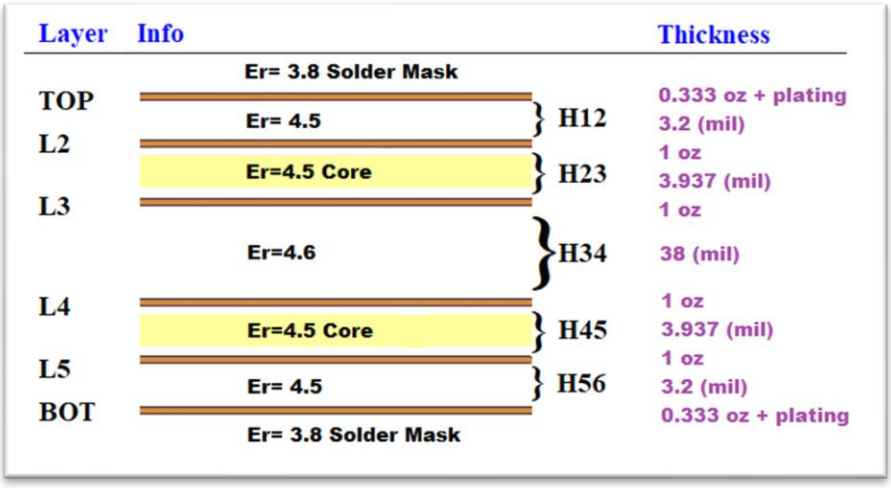
4.4. CA Bus



- All signals use point-to-point routing topology, except CKE and RSTn.
- Refer to the EVK layout for the placement of the CKE pull-down resistor and the RSTn pull-up resistor.
- CLK must be routed in pairs on the same layer to match the propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- The total trace length (L0 + L1) is recommended to be no longer than 1200 mils to minimize attenuation.
- For each CA channel, the length matching for CA(CS) to CA(CS) (Lp + L0 + L1) should be within +/-20ps.
- For each CA channel, the length matching for CLK to CA(CS) (Lp + L0 + L1) should be within +/-25ps.
- For each CA channel, the length matching for CLKp to CLKn (Lp + L0 + L1) should be within +/-0.5ps.
- For each CA channel, the length matching for CLK to DQS (Lp + L0 + L1) should be within +/-60ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between differential signal (CLKp / CLKn) to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

4.5. Board 6-Layers Stack up

- The Synaptics EVK (Evaluation Kit) board uses the most common 1.6mm PCB stack-up shown below.
- It is suggested that H34 be more than 5x the thickness of H23/H45 to avoid cross talk between signals on L3 and L4.
- High-speed data signals that run on the top layer(L3) should reference L2 (VSS).
- Low-speed CA signals that run on the bottom layer (L4) should reference L5 (PWR).



- For customers concerned about EMI, Synaptics has explored another layout strategy which all signals running on the inner layers (L3 and L4):
  - L3 refers to L2 (VSS) as the reference plane
  - L4 refers to L5 (PWR) as the reference plane.
- With limited routing space, some data signals may need to run on L4, which can result in worse signal integrity (SI) due to plated through-hole (PTH) vias and long return paths. To minimize the side effects of routing on L4, the thickness of H34 (the dielectric layer between L3 and L4) needs to be reduced.

5. Revision History

Revision	Description
A	Initial Release
B	Release as public document.
C	Added the following sections: • 1 PCB Layout Guidelines • 2 Power Supply Guidelines • 3 4L non-HDI PCB Design Rules
D	Minor update to document title.
E	Minor update to latest template.

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