SL1640 Embedded IoT Processor

Electrical Specification Datasheet

Overview

The Synaptics SL-Series of embedded processors is a family of highly integrated AI-native Linux® and Android™ SoCs optimized for multi-modal consumer, enterprise, and industrial IoT workloads with hardware accelerators for edge inferencing, security, video, graphics, and audio.

The Synaptics SL1640 SoC incorporates multiple high-performance compute engines including a quad-core Arm® Cortex®-55 CPU subsystem, multi-TOPS NPU, GPU for AI-acceleration and 3D graphics, along with dual-core DSP, 4K video decoder and 1080p encoder, backed by industry-grade security certifications.

The SL1640 supports the Synaptics® Astra™ IoT platform, delivering a unified experience through standards-based approaches, open software frameworks, full-featured AI toolkits, and market-ready evaluation systems.

In combination with Synaptics' best-in-class wireless connectivity portfolio, the SL1640 enables cost-optimized system solutions with performance-per-watt benefits for the IoT.

Features

Processors

- Quad-Core Arm Cortex-A55 processor with Cryptographic Extensions
- Up to 2.0 GHz for each CPU, delivering up to 24K DMIPS
  - With dynamic voltage and frequency scaling
- Each processor has 32KB I-cache and 32KB D-Cache
- Each processor has dedicated Arm NEON™ technology/VFPU
  - 32 128-bit SIMD registers, crypto instructions
- 64 KB per core L2 Cache and 512KB shared L3 Cache
- Arm CoreSight™ technology-compatible debugging interface
- TrustZone® technology with Synaptics TEE Software
- Supports standard tool chains (ARM, GNU)

Memory Interface

- DRAM controller
  - 32-bit DDR4-3200, LPDDR4/LPDDR4x-3733 (see Note:)
  - Up to 4 GB memory space
  - Supports out-of-order issue of transactions to maximize DRAM utilization rate
  - Secure control

Note: Supports only single RANK for LPDDR4/LPDDR4x device.

- eMMC 5.1 Controller
  - x1, x4 or x8-bit interface

Neural Processing Unit

- Dedicated hardware for localized NN/machine learning applications
  - Up to 1.6+ TOPS
- Support for TensorFlow® Lite, Android™ NN API, and OpenVX™
- OVX and NBG outputs of SyNAP™ toolkit support
- MMU
- AI use case examples:
  - Content/channel logo detection
  - Parental control
  - Custom wake words
  - Auto-ducking
  - Vision use cases such as Face ID

Digital Signal Processor

- Cadence® Tensilica® Dual HiFi 4

Video Encoding / Decoding

- Video encoding
  - H.264
  - Single 1080p30 8-bit
- Video decoding
  - AV1 Main profile
  - H.265 Main profile, Main10 profile
  - H.264 Baseline, Main and High profiles
  - VP9 Profiles 0 and 2
  - VP8
  - MPEG-2 Simple and Main Profiles
  - Simultaneous 2160p60 10-bit and 1080p60 10-bit streams
- Able to run as secure master or non-secure master, with software driver inside Synaptics TEE

Audio Decoding/Processing

- Far Field Voice (FFV) processing supporting Automatic Speech Recognition (ASR) and Communication & Keyword Detection
- Microphone(s) input processing
- Audio decompression of various formats
- Audio post-processing

2D & 3D Graphics

- Imagination™ PowerVR™ Series9XE GE9608 GPU
  - OpenGL® ES™ 1.1/2.0/3.0/3.1/3.2/ OpenCL™ 1.2 / Vulkan® 1.1
  - Android™ NN API through IMGDNN API

Video/Graphics Display Pipeline with QDEO™

- Display path:
  - Output after MP/GFX0/GFX1 overlay
  - Output through HDMI Tx (up to 2160p60) / DSI (up to 2160p30)
  - Supports gamma correction and low-latency mode (for both source/sink devices)

- MP:
  - Scaling up and scaling down
  - Detail and edge enhancement
  - Flesh tone detection
  - Luma transition improvement
  - Chroma transition improvement
  - Adaptive contrast enhancement
  - Intelligent color re-mapper (chroma enhancement)
  - 90/180/270 rotation
  - Horizontal and vertical flip
  - Gamma correction
- GFX0/GFX1:
  - Scaling up only
- Offline video pipeline (OVP):
  - Offline deinterlacer
  - Offline scalar

Security

- Completely firewalled Security Processor
- Secure Boot
- Arm TrustZone® support
- Disable / enable JTAG through authentication
- Memory and I/O space access control
- DRAM scrambling support
- SmartCard
- HDCP 2.3
- SyKure™ – Secure AI inferencing

Audio / Video Outputs

- One HDMI v2.1 output
  - 3840x2160 60Hz 12-bit
- MIPI-DSI 1.2
  - 4 lanes
  - 3840x2160 30Hz 10-bit (max resolution)
  - 1920x1080 60Hz
- I^2S audio output, 4 stereo interfaces capable of 8 channel TDM
- S/PDIF output

Audio / Video Inputs

- Transport Stream
  - 8 Serial TS inputs
    - Each input can support two multiplexed streams (double-speed interface) up to 8 streams total @512 Mbps per stream max
  - 256 PID filters
  - 128 section filters
  - 12-byte section header filtering

- I^2S audio input, 4 stereo interfaces capable of 8 channel TDM
- PDM, two stereo interfaces supporting up to four microphones
- S/PDIF input
- PCM audio I/O interface compatible with I^2S and TDM

Standby Domain Manager (System Manager)

- SM CPU
- 2-input auxiliary ADC
- Two timers
- Always-on domain to support system wake-up events:
  - Wake-on-LAN with on-chip FE PHY
  - Wake-on-X (Wi-Fi, BT, ZigBee) via GPIO

Peripherals

- Fast Ethernet MAC/PHY
  - 10/100 MAC is only available to the in-built FE PHY
- One USB 2.0 On-The-Go (OTG) interface
- One USB 3.0 Host
- PCIe Gen2 single lane, Root-Complex
- One SDIO 3.01 host interface up to 200 MHz, 1.8V only
- Four TWSI 2-wire bus (I^2C compatible)
- One high-speed UART interface
- Two low-speed UART interfaces (in always-on power domain)
- Two SPI interfaces (one with DMA)
- 20-bit GPIOs (SM)
- 67-bit GPIOs (SoC)
- Four PWM
- 2-input auxiliary ADC
- SmartCard
- On chip temperature sensor

Power, Package and Layout

- Package: 13mm x 13mm FCBGA, 0.4mm ball pitch
  - Ball pattern supports standard PCB fab rules (no HDI rules required)

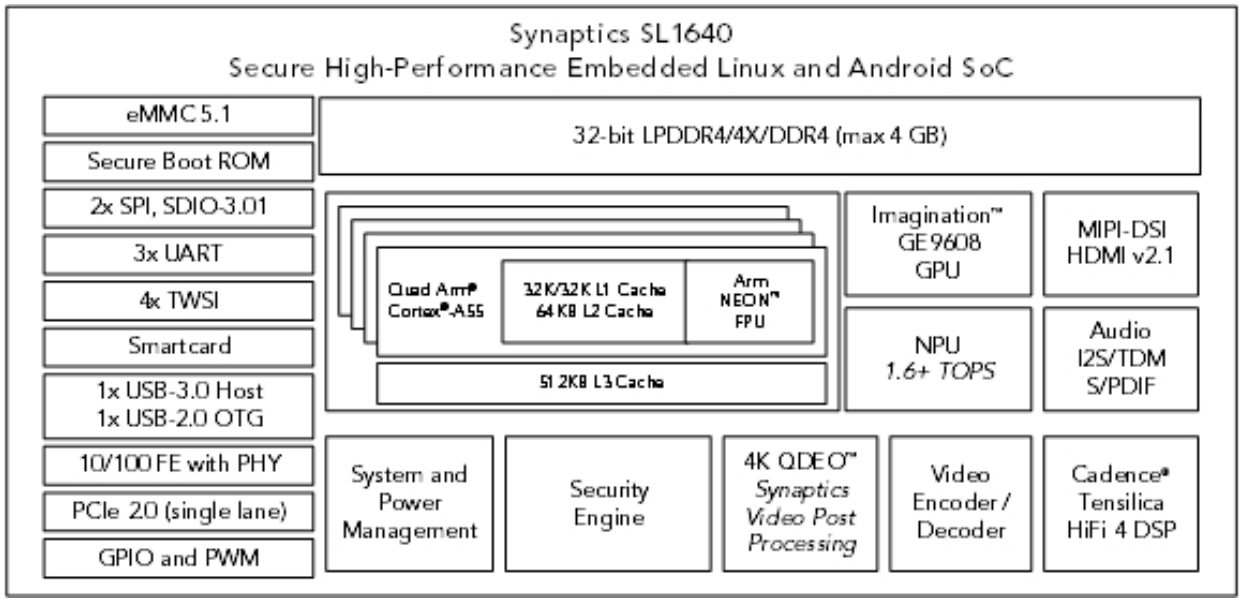

Figure 1. SL1640 high-level block diagram

Related Content

These document are associated with the SL1640.

Part Number	Document Title
505-001416-01	SL1640 Functional Specification A functional specification of the SL1640 device core.
506-001443-01	Synaptics General Guide for Soldering SMD to PC Boards Application Note
506-001454-01	Synaptics General ESD/EOS Control Methods Application Note

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1. Signal Description

Table 1. Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
I/O	Input and output
Analog	Analog Pin
CMOS	Complementary metal oxide semiconductor
SSTL	Stub Series Terminated Logic
PWR	Power Supply
GND	Ground Pin
Iu	Input with internal pull-up
Id	Input with internal pull-down
I/Ood	Input/Output pin, Open-Drain type
I/Ouod	Input/Output pin with internal pull-up, Open-Drain type
I/Odod	Input/Output pin with internal pull-down, Open-Drain type
Ouod	Output pin with internal pull-up, Open-Drain type
Ou	Output pin with internal pull-up
Od	Output pin with internal pull-down

Note: A lowercase n at the end of a signal name indicates an active-low signal.

Table 2. Interface Prefixes

Pin Type	Definitions
TWSI	TW_
System Manager	SM_
DDR4/LPDDR4 memory channel 0, 1, 2, 3	M0_, M1_, M2_, M3_
Serial transport stream interface	STS0_, STS1_

1.1. SL1640 Pinout

Due to the large number of pins, the package is depicted graphically over the following 4 pages.

Table 3. SL1640 Pinouts Top View (1 of 4)

	1	2	3	4	5	6	7	8	9	
A	VSS	VSS		VDD_CPU_FB		STS0_VALD		STS1_SOP		A
B	VSS	VSS		VSS	STS0_CLK	STS0_SOP	STS0_SD	STS1_CLK		B
C	M0_DQ[23]	M0_DQ[21]	M0_DQSp[2]	M0_DQSn[2]			VSS	CPUPLL_AVDD1P8		C
D		M0_DQ[17]		M0_DQ[22]	VSS	GPIO_A[2]		VSS		D
E	M0_DM[2]	M0_DQ[19]				MEMPLL_AVDD1P8			CPUTSEN_AVDD1P8	E
F		M0_DQ[31]	VSS	M0_DQ[18]		VSS		VSS		F
G		M0_DQSn[3]						VSS		G
H	M0_DQ[25]	M0_DQSp[3]	VSS	M0_DQ[20]		M0_DQ[16]	VSS			H
J		M0_DM[3]								J
K	M0_DQ[29]	M0_DQ[27]	VSS	M0_DQ[28]		M0_DQ[24]	VSS			K
L	VSS	M0_ACTn		M0_DQ[26]					VSS	L
M		M0_RASn		VSS		M0_DQ[30]	VSS		VDDQ	M
N	M0_A[1]	M0_A[5]	VSS	M0_A[10]						N
P		M0_WEn	VSS	M0_CSn		M0_A[4]	M0_ODT		VDDQ	P
R	M0_CKE	M0_A[6]							VSS	R
T		M0_CASn	M0_A[8]	M0_BA[0]		VSS	M0_BA[1]			T
U									VDDQ	U
V	M0_A[2]	M0_BG	M0_A[7]	VSS		M0_A[3]	M0_CAL			V
W		M0_A[9]	M0_A[12]						VDDQ	W
Y	M0_CKp	M0_CKn	VSS	M0_A[0]		VSS	M0_DQ[2]			Y
AA		VSS							VSS	AA
AB		M0_A[11]	M0_DQ[4]	VSS		M0_DQ[6]	VSS			AB
AC	M0_A[13]	M0_RSTn								AC
AD		M0_DQSn[0]	VSS	M0_DQ[1]		VSS	VSS		M0_AVDD1P8	AD
AE	M0_DQ[0]	M0_DQSp[0]								AE
AF	M0_DM[0]	M0_DQ[7]	VSS	M0_DQ[12]		M0_DQ[8]	VSS		I2S2_MCLK	AF
AG		M0_DQ[3]					I2S3_DI		I2S2_DI[3]	AG
AH	M0_DQ[5]	M0_DM[1]		M0_DQ[14]		VSS				AH
AJ		M0_DQ[11]		M0_DQ[10]	VSS		I2S3_DO		I2S2_DI[0]	AJ
AK	M0_DQSp[1]	M0_DQSn[1]					HDMI_TX_EDDC_SDA		I2S2_DI[1]	AK
AL	VSS	VSS	M0_DQ[9]	M0_DQ[13]	I2S3_BCLK	I2S3_LRCK	HDMI_TX_EDDC_SCL	I2S1_MCLK		AL
AM	VSS	VSS	M0_DQ[15]		VSS			I2S2_DI[2]		AM
	1	2	3	4	5	6	7	8	9	

Table 4. SL1640 Pinouts Top View (2 of 4)

	10	11	12	13	14	15	16	17	18	
A	SPI1_SS1n			SPI1_SDO		SDIO0_CDn			EMMC_DATA[4]	A
B	SPI1_SS0n		SPI1_SS3n	SPI1_SS2n	SPI1_SCLK	SPI1_SDI		EMMC_DATA[6]	EMMC_DATA[5]	B
C	STS1_SD	STS1_VALD			VDDIO1P8	SDIO0_WP		EMMC_DATA[7]		C
D			VDDIO1P8		VSS				EMMC_RSTn	D
E							SYSPLL_AVDD1P8			E
F	GPIO_A[1]		VSS		TWO_SDA		VSS		EMMC_DATA[1]	F
G	VSS		GPIO_A[0]		TWO_SCL		USB2_DRV_VBUS		EMMC_DATA[2]	G
H										H
J	VSS		VSS		VSS		VSS		VSS	J
K	VSS		VSS		VDD_CPU		VDD_CPU		VSS	K
L	VSS		VSS							L
M	VDDQ		VDDQLP		VDD_CPU		VDD_CPU		VDD_CORE	M
N			VDDQLP	VSS	VSS		VDD_CPU		VSS	N
P	VDDQ		VSS		VDD_CPU		VDD_CPU		VDD_CORE	P
R	VSS		VSS							R
T			VDDQLP		VDD_CORE		VSS		VSS	T
U	VSS				VSS		VDD_CORE		VDD_CORE	U
V		VSS	VDDQLP							V
W					VSS		VDD_CORE		VSS	W
Y		VDDQLP	VDDQLP		VDD_CORE		VSS		VDD_CORE	Y
AA			VSS		VSS		VDD_CORE		VSS	AA
AB	VDD_CORE									AB
AC					VDD_CORE		VSS		VDD_CORE	AC
AD	VSS		VSS		VSS		VDD_CORE		VDD_CORE	AD
AE										AE
AF		VSS		I2S2_BCLK		VSS	VSS	HDMI_TX_AVDD		AF
AG		I2S2_LRCK		VSS		MIPI_DSI_AVDD			HDMI_TX_AVDD1P8	AG
AH						MIPI_DSI_AVDD1P8				AH
AJ		VSS		KILOOTP_AVDD1P8		VDDIO1P8				AJ
AK	SPDIFI	I2S1_LRCK		I2S1_DO[3]	VSS			VSS		AK
AL	SPDIFO	I2S1_DO[2]		I2S1_DO[0]	MIPI_DSI_REXT	MIPI_DSI_CKp	MIPI_DSI_D0p	MIPI_DSI_D0n	MIPI_DSI_D1p	AL
AM	I2S1_BCLK			I2S1_DO[1]		MIPI_DSI_CKn			MIPI_DSI_D1n	AM
	10	11	12	13	14	15	16	17	18	

Table 5. SL1640 Pinouts Top View (3 of 4)

	19	20	21	22	23	24	25	26	
A		EMMC_DATA[3]			SDIO0_DATA[1]		USB2_Dn	USB2_VBUS	A
B	EMMC_STRB	EMMC_CLK		SDIO0_DATA[0]	SDIO0_CMD	USB2_ID	USB2_Dp	USB2_REXT	B
C		EMMC_CMD	SDIO0_VDDIO1P8	SDIO0_DATA[2]				USB2_AVDD3P3	C
D		EMMC_DATA[0]		SDIO0_CLK	USB2_VR_AVDD3P3	VSS		VSS	D
E									E
F		VSS		SDIO0_DATA[3]		USB2_DVDD		VSS	F
G		EMMC_VDDIO1P8		VSS		VSS		VSS	G
H									H
J		VSS		VSS		VSS		PCIE_PLL_AVSS	J
K		VSS		VSS		VSS		PCIE_PLL_AVDD1P8	K
L		VSS						VSS	L
M		VDD_CORE		VSS		VSS			M
N				VDD_CORE		VDD_CORE		VSS	N
P		VDD_CORE	VSS	VSS		VSS			P
R								SM_ADC_AVSS	R
T		VDD_CORE		VDD_CORE		VSS			T
U		VSS		VSS		VSS		VSS	U
V									V
W		VDD_CORE		VSS		VSS		VSS	W
Y		VSS		VDD_CORE		VSS			Y
AA		VDD_CORE		VSS		VDD_CORE		SM_FE_AVSS	AA
AB									AB
AC		VSS		VDD_CORE		VSS		SM_TDI	AC
AD		VDD_CORE		VSS		VDD_CORE			AD
AE								VSS	AE
AF	VSS		VSS		VSS		VSS		AF
AG	HDMI_TX_REXT		HDMI_TX_HPD		AVPLL_AVDD1P8		SM_SPI2_SCLK		AG
AH									AH
AJ			VSS		VDD_CORE_FB		VSS		AJ
AK	VSS			VSS			VSS		AK
AL	MIPI_DSI_D3p	MIPI_DSI_D3n	MIPI_DSI_D2n		HDMI_TX_CKn	HDMI_TX_D0n	HDMI_TX_D0p	HDMI_TX_D1n	AL
AM			MIPI_DSI_D2p		HDMI_TX_CKp			HDMI_TX_D1p	AM
	19	20	21	22	23	24	25	26	

Table 6. SL1640 Pinouts Top View (4 of 4)

	27	28	29	30	31	32	
A		USB3_VBUS		USB3_Dp	VSS	VSS	A
B		USB3_ID	USB3_REXT	USB3_Dn	VSS	VSS	B
C			USB3_AVDD		USB3_RXp	USB3_RXn	C
D	USB3_AVDD3P3		USB3_DVDD				D
E					USB3_TXn	USB3_TXp	E
F		PCIE_TX_AVDD		PCIE_AVDD1P8	PCIE_TX0p	VSS	F
G					PCIE_TX0n		G
H		VSS		PCIE_RX0n	PCIE_RX0p		H
J		PCIE_AVDD		VSS			J
K				PCIE_CLKp	PCIE_CLKn		K
L					PCIE_REXT		L
M		VSS	PCIE_REFCLK_AVDD		SCRD0_RST	SCRD0_DCLK	M
N	VDDIO1P8		VSS		SCRD0_CRD_PRES		N
P			SM_ADC_AVDD1P8		SCRD0_DIO	VSS	P
R	SM_ADCI[0]	SM_ADCI[1]		VSS	SM_RCLKO	SM_RCLKI	R
T							T
U	SM_OSC_VDDIO1P8		VSS	VSS	SM_FE_ATB_A	SM_FE_ATB_B	U
V				SM_FE_RXn			V
W	SM_TSEN_AVDD1P8		VSS	SM_FE_RXp			W
Y			SM_FE_AVDD	SM_FE_TXn	SM_FE_TXp		Y
AA	SM_FE_AVDD1P8		VSS	SM_FE_AVDD3P3	SM_FE_RSET	VSS	AA
AB					SM_TW2_SCL		AB
AC	SM_VDD_CORE		VSS		SM_TW2_SDA	SM_URT1_TXD	AC
AD				SM_POR_EN	SM_URT1_RXD		AD
AE	SM_TEST_EN		SM_JTAG_SEL	SM_RSTIn	SM_HDMI_TX_CEC	SM_HDMI_TX_HPD	AE
AF							AF
AG	VSS		SM_TDO	SM_TRSTn	SM_TCK		AG
AH					SM_TW3_SCL	SM_TMS	AH
AJ	SM_VDDIO1P8	VSS		SM_SPI2_SS0n	SM_TW3_SDA		AJ
AK		SM_URT0_RXD			SM_SPI2_SS1n	SM_SPI2_SS2n	AK
AL	HDMI_TX_D2p	SM_URT0_TXD	SM_SPI2_SDI	SM_SPI2_SS3n	VSS	VSS	AL
AM	HDMI_TX_D2n			SM_SPI2_SDO	VSS	VSS	AM
	27	28	29	30	31	32	

1.2. Pin Descriptions

Table 7. DDR4 M0 Interface Configuration (Sheet 1 of 3)

Pin #	Pin Name	Pin Type	Description
AC2	M0_RSTn	O, SSTL12	M0 RESETn for DDR4 SDRAMs. This pin is active low.
Y2	M0_CKn	O, SSTL12	M0 CK0n for 2 x16 chips.
Y1	M0_CKp	O, SSTL12	M0 CK0p for 2 x16 chips.
R1	M0_CKE	O, SSTL12	M0 Clock enable.
P7	M0_ODT	O, SSTL12	M0 On die termination.
P4	M0_CSn	O, SSTL12	M0 Chip select.
M2	M0_RASn	O, SSTL12	M0 Row activate.
T2	M0_CASn	O, SSTL12	M0 Column activate.
P2	M0_WEn	O, SSTL12	M0 Write enable.
T4	M0_BA[0]	O, SSTL12	M0 Bank select[0].
T7	M0_BA[1]	O, SSTL12	M0 Bank select[1].
L2	M0_ACTn	O, SSTL12	M0 ACTn.
V2	M0_BG	O, SSTL12	M0 Bank Group.
Y4	M0_A[0]	O, SSTL12	DDR4_M0_A0.
N1	M0_A[1]	O, SSTL12	DDR4_M0_A1.
V1	M0_A[2]	O, SSTL12	DDR4_M0_A2.
V6	M0_A[3]	O, SSTL12	DDR4_M0_A3.
P6	M0_A[4]	O, SSTL12	DDR4_M0_A4.
N2	M0_A[5]	O, SSTL12	DDR4_M0_A5.
R2	M0_A[6]	O, SSTL12	DDR4_M0_A6.
V3	M0_A[7]	O, SSTL12	DDR4_M0_A7.
T3	M0_A[8]	O, SSTL12	DDR4_M0_A8.
W2	M0_A[9]	O, SSTL12	DDR4_M0_A9.
N4	M0_A[10]	O, SSTL12	DDR4_M0_A10.
AB2	M0_A[11]	O, SSTL12	DDR4_M0_A11.
W3	M0_A[12]	O, SSTL12	DDR4_M0_A12.
AC1	M0_A[13]	O, SSTL12	DDR4_M0_A13.
AF1	M0_DM[0]	I/O, POD12	M0 Data mask BYTE[0].
AH2	M0_DM[1]	I/O, POD12	M0 Data mask BYTE[1].
E1	M0_DM[2]	I/O, POD12	M0 Data mask BYTE[2].
J2	M0_DM[3]	I/O, POD12	M0 Data mask BYTE[3].
AE1	M0_DQ[0]	I/O, POD12	DDR4_M0_DQ0.

Table 7. DDR4 M0 Interface Configuration (Sheet 2 of 3)

Pin #	Pin Name	Pin Type	Description
AD4	M0_DQ[1]	I/O, POD12	DDR4_M0_DQ1.
Y7	M0_DQ[2]	I/O, POD12	DDR4_M0_DQ2.
AG2	M0_DQ[3]	I/O, POD12	DDR4_M0_DQ3.
AB3	M0_DQ[4]	I/O, POD12	DDR4_M0_DQ4.
AH1	M0_DQ[5]	I/O, POD12	DDR4_M0_DQ5.
AB6	M0_DQ[6]	I/O, POD12	DDR4_M0_DQ6.
AF2	M0_DQ[7]	I/O, POD12	DDR4_M0_DQ7.
AF6	M0_DQ[8]	I/O, POD12	DDR4_M0_DQ8.
AL3	M0_DQ[9]	I/O, POD12	DDR4_M0_DQ9.
AJ4	M0_DQ[10]	I/O, POD12	DDR4_M0_DQ10.
AJ2	M0_DQ[11]	I/O, POD12	DDR4_M0_DQ11.
AF4	M0_DQ[12]	I/O, POD12	DDR4_M0_DQ12.
AL4	M0_DQ[13]	I/O, POD12	DDR4_M0_DQ13.
AH4	M0_DQ[14]	I/O, POD12	DDR4_M0_DQ14.
AM3	M0_DQ[15]	I/O, POD12	DDR4_M0_DQ15.
H6	M0_DQ[16]	I/O, POD12	DDR4_M0_DQ16.
D2	M0_DQ[17]	I/O, POD12	DDR4_M0_DQ17.
F4	M0_DQ[18]	I/O, POD12	DDR4_M0_DQ18.
E2	M0_DQ[19]	I/O, POD12	DDR4_M0_DQ19.
H4	M0_DQ[20]	I/O, POD12	DDR4_M0_DQ20.
C2	M0_DQ[21]	I/O, POD12	DDR4_M0_DQ21.
D4	M0_DQ[22]	I/O, POD12	DDR4_M0_DQ22.
C1	M0_DQ[23]	I/O, POD12	DDR4_M0_DQ23.
K6	M0_DQ[24]	I/O, POD12	DDR4_M0_DQ24.
H1	M0_DQ[25]	I/O, POD12	DDR4_M0_DQ25.
L4	M0_DQ[26]	I/O, POD12	DDR4_M0_DQ26.
K2	M0_DQ[27]	I/O, POD12	DDR4_M0_DQ27.
K4	M0_DQ[28]	I/O, POD12	DDR4_M0_DQ28.
K1	M0_DQ[29]	I/O, POD12	DDR4_M0_DQ29.
M6	M0_DQ[30]	I/O, POD12	DDR4_M0_DQ30.
F2	M0_DQ[31]	I/O, POD12	DDR4_M0_DQ31.
AD2	M0_DQSn[0]	I/O, POD12	DDR4_M0_DQS0n.
AE2	M0_DQSp[0]	I/O, POD12	DDR4_M0_DQS0p.
AK2	M0_DQSn[1]	I/O, POD12	DDR4_M0_DQS1n.

Table 7. DDR4 M0 Interface Configuration (Sheet 3 of 3)

Pin #	Pin Name	Pin Type	Description
AK1	M0_DQSp[1]	I/O, POD12	DDR4_M0_DQS1p.
C4	M0_DQSn[2]	I/O, POD12	DDR4_M0_DQS2n.
C3	M0_DQSp[2]	I/O, POD12	DDR4_M0_DQS2p.
G2	M0_DQSn[3]	I/O, POD12	DDR4_M0_DQS3n.
H2	M0_DQSp[3]	I/O, POD12	DDR4_M0_DQS3p.

Table 8. USB2.0 Interface

Pin Location(s)	Signal	Pin Type	Description
B25	USB2_Dp	I/O, Analog	USB 2.0 port data positive.
A25	USB2_Dn	I/O, Analog	USB 2.0 port data negative.
G16	USB2_DRV_VBUS	O, CMOS	USB OTG requires this signal. It enables 5V to be driven onto VBUS. 0 = Do not drive VBUS. 1 = Drive 5V on VBUS. DRV_VBUS must be connected to an external PMIC chip to provide power for USB VBUS. There is no on-chip power switch for VBUS inside the PHY.
B24	USB2_ID	I, Analog	USB 2.0 Port OTG ID pin. This pin should be left floating or connected to GND.
B26	USB2_REXT	I, Analog	USB 2.0 Calibration pad. This pin should be connected to VSS via a 200 Ohm resistor.
A26	USB2_VBUS	I, Analog	USB 2.0 VBUS. This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30 kOhm resistor so it could see a lower voltage.

Table 9. USB3.0 Interface

Pin Location(s)	Signal	Pin Type	Description
A30	USB3_Dp	I/O, Analog	USB 3.0 port data positive.
B30	USB3_Dn	I/O, Analog	USB 3.0 port data negative.
B28	USB3_ID	I, Analog	USB 3.0 port 0 ID pin. This pin should be left floating or connected to GND.
B29	USB3_REXT	I, Analog	USB 3.0 Calibration pad. This pin should be connected to VSS via a 200 ohm resistor.
C31	USB3_RXp	I, Analog	USB 3.0 port receive positive.
C32	USB3_RXn	I, Analog	USB 3.0 port receive negative.
E32	USB3_TXp	O, Analog	USB 3.0 port transmit positive.
E31	USB3_TXn	O, Analog	USB 3.0 port transmit negative.
A28	USB3_VBUS	I, Analog	USB 3.0 port 0 VBUS. This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30 kOhm resistor so it could see a lower voltage.

Table 10. HDMI Transmitter PHY Interface

Pin Location(s)	Signal	Pin Type	Description
AG19	HDMI_TX_REXT	I, Analog	HDMI TX Calibration pad. This pin should be connected to VSS via a 1.62K Ohm resistor.
AG21	HDMI_TX_HPD	I, CMOS	HDMI TX hot plug detect. This pin is 5V tolerant. 1=Detect.
AL23	HDMI_TX_CKn	O, Analog	TMDS clock negative.
AM23	HDMI_TX_CKp	O, Analog	TMDS clock positive.
AL24	HDMI_TX_D0n	O, Analog	TMDS data 0 negative.
AL25	HDMI_TX_D0p	O, Analog	TMDS data 0 positive.
AL26	HDMI_TX_D1n	O, Analog	TMDS data 1 negative.
AM26	HDMI_TX_D1p	O, Analog	TMDS data 1 positive.
AM27	HDMI_TX_D2n	O, Analog	TMDS data 2 negative.
AL27	HDMI_TX_D2p	O, Analog	TMDS data 2 positive.

Table 11. HDMI TX Enhanced DDC Interface

Pin Location(s)	Signal	Pin Type	Description
AL7	HDMI_TX_EDDC_SCL	IOod, CMOS	HDMI TX DDC serial clock line. This pin is 1.8V-only.
AK7	HDMI_TX_EDDC_SDA	IOod, CMOS	HDMI TX DDC serial data line. This pin is 1.8V-only.

Table 12. Serial Transport 0 Interface

Pin Location(s)	Signal	Pin Type	Description
B5	STS0_CLK	I, CMOS	Serial TS capture serial data clock.
B7	STS0_SD	I, CMOS	Serial TS capture serial data.
B6	STS0_SOP	I, CMOS	Serial TS capture start of packet.
A6	STS0_VALD	I, CMOS	Serial TS capture valid flag.

Table 13. Serial Transport 1 Interface

Pin Location(s)	Signal	Pin Type	Description
B8	STS1_CLK	I, CMOS	Serial TS capture serial data clock.
C10	STS1_SD	I, CMOS	Serial TS capture serial data.
A8	STS1_SOP	I, CMOS	Serial TS capture start of packet.
C11	STS1_VALD	I, CMOS	Serial TS capture valid flag.

Table 14. Smart Card Interface

Pin Location(s)	Signal	Pin Type	Description
N31	SCRD0_CRD_PRES	I, CMOS	Card 0 presence detect.
M32	SCRD0_DCLK	O, CMOS	Card 0 clock.
P31	SCRD0_DIO	I/O, CMOS	Card 0 Data.
M31	SCRD0_RST	O, CMOS	Card 0 Reset.

Table 15. Audio I²S Interface and S/PDIF Output

Pin Location(s)	Signal	Pin Type	Description
AM10	I2S1_BCLK	I/O, CMOS	Audio bit clock.
AL13	I2S1_DO[0]	O, CMOS	Data output.
AM13	I2S1_DO[1]	O, CMOS	Data output.
AL11	I2S1_DO[2]	O, CMOS	Data output.
AK13	I2S1_DO[3]	O, CMOS	Data output.
AK11	I2S1_LRCK	I/O, CMOS	Audio WS or LR select.
AL8	I2S1_MCLK	I/O, CMOS	MCLK input/output.

Table 16. Audio I²S and S/PDIF Interface

Pin Location(s)	Signal	Pin Type	Description
AF13	I2S2_BCLK	I/O, CMOS	Audio bit clock.
AJ9	I2S2_DI[0]	I, CMOS	Data input.
AK9	I2S2_DI[1]	I, CMOS	Data input.
AM8	I2S2_DI[2]	I, CMOS	Data input.
AG9	I2S2_DI[3]	I, CMOS	Data input.
AG11	I2S2_LRCK	I/O, CMOS	Audio WS or LR select.
AF9	I2S2_MCLK	O, CMOS	MCLK output.
AK10	SPDIFI	I, CMOS	S/PDIF input.
AL10	SPDIFO	O, CMOS	S/PDIF output.

Table 17. Audio I²S Interface 3

Pin Location(s)	Signal	Pin Type	Description
AL5	I2S3_BCLK	I/O, CMOS	Audio bit clock.
AG7	I2S3_DI	I, CMOS	Data input.
AJ7	I2S3_DO	O, CMOS	Data output.
AL6	I2S3_LRCK	I/O, CMOS	Audio WS or LR select.

Table 18. DDR4/LPDDR4/LPDDR4x Calibration

Pin Location(s)	Signal	Pin Type	Description
V7	M0_CAL	I, Analog	DDR4/LPDDR4/LPDDR4x Calibration pin. Connect to VSS (DDR4) or 1.1V VDDQ (LPDD4/4X) via a 120 Ohm ±1% resistor.

Table 19. SoC Two-Wire Serial Interface

Pin Location(s)	Signal	Pin Type	Description
G14	TW0_SCL	I/Ood, CMOS	TWSI serial clock.
F14	TW0_SDA	I/Ood, CMOS	TWSI serial data.

Table 20. SoC SPI Interface

Pin Location(s)	Signal	Pin Type	Description
B10	SPI1_SS0n	O, CMOS	SPI1 chip select 0 for first slave device with handler.
A10	SPI1_SS1n	O, CMOS	SPI1 chip select 1 for second slave device with handler.
B13	SPI1_SS2n	O, CMOS	SPI1 chip select 2 for third slave device.
B12	SPI1_SS3n	O, CMOS	SPI1 chip select 3 for fourth slave device.
B14	SPI1_SCLK	O, CMOS	SPI1 serial clock.
B15	SPI1_SDI	I, CMOS	SPI1 serial data input.
A13	SPI1_SDO	O, CMOS	SPI1 serial data output.

Table 21. PCI Express 2.0 Interface

Pin Location(s)	Signal	Pin Type	Description
K30	PCIE_CLKp	O, Analog	PCIe RefClk positive.
K31	PCIE_CLKn	O, Analog	PCIe RefClk negative.
L31	PCIE_REXT	I, Analog	PCIe Reference resistor connection. Connect to VSS via a 200 ohm resistor.
H31	PCIE_RX0p	I, Analog	PCIe 0 receive positive.
H30	PCIE_RX0n	I, Analog	PCIe 0 receive negative.

Table 21. PCI Express 2.0 Interface

Pin Location(s)	Signal	Pin Type	Description
F31	PCIE_TX0p	O, Analog	PCIe 0 transmit positive.
G31	PCIE_TX0n	O, Analog	PCIe 0 transmit negative.

Table 22. eMMC Interface

Pin Location(s)	Signal	Pin Type	Description
B20	EMMC_CLK	O, CMOS	Output clock.
D18	EMMC_RSTn	O, CMOS	Hardware reset.
B19	EMMC_STRB	I, CMOS	eMMC 5.0 data strobe.
D20	EMMC_DATA[0]	I/O, CMOS	Data[0].
F18	EMMC_DATA[1]	I/O, CMOS	Data[1].
G18	EMMC_DATA[2]	I/O, CMOS	Data[2].
A20	EMMC_DATA[3]	I/O, CMOS	Data[3].
A18	EMMC_DATA[4]	I/O, CMOS	Data[4].
B18	EMMC_DATA[5]	I/O, CMOS	Data[5].
B17	EMMC_DATA[6]	I/O, CMOS	Data[6].
C17	EMMC_DATA[7]	I/O, CMOS	Data[7].
C20	EMMC_CMD	I/O, CMOS	Command/Response.

Table 23. SDIO Interface

Pin Location(s)	Signal	Pin Type	Description
A15	SDIO0_CDn	I, CMOS	Card Detect. 0 = Detect.
D22	SDIO0_CLK	O, CMOS	Output clock. CLK in SPI mode.
B23	SDIO0_CMD	I/O, CMOS	Command/Response. DO in SPI mode.
B22	SDIO0_DATA[0]	I/O, CMOS	Data[0], busy from card. DI in SPI mode.
A23	SDIO0_DATA[1]	I/O, CMOS	Data[1]. Int from card.
C22	SDIO0_DATA[2]	I/O, CMOS	Data[2]. Read wait from card.
F22	SDIO0_DATA[3]	I/O, CMOS	Data[3]. SSn in SPI mode.
C15	SDIO0_WP	I, CMOS	Write Protect. 1= Write-protected.

Table 24. MIPI Display Serial Interface Pins

Pin Location(s)	Signal	Pin Type	Description
AL15	MIPI_DSI_CKp	O, Analog	MIPI DSI CLK positive.
AM15	MIPI_DSI_CKn	O, Analog	MIPI DSI CLK negative.
AL16	MIPI_DSI_D0p	O, Analog	MIPI DSI Data Lane 0 positive.
AL17	MIPI_DSI_D0n	O, Analog	MIPI DSI Data Lane 0 negative.
AL18	MIPI_DSI_D1p	O, Analog	MIPI DSI Data Lane 1 positive.
AM18	MIPI_DSI_D1n	O, Analog	MIPI DSI Data Lane 1 negative.
AM21	MIPI_DSI_D2p	O, Analog	MIPI DSI Data Lane 2 positive.
AL21	MIPI_DSI_D2n	O, Analog	MIPI DSI Data Lane 2 negative.
AL19	MIPI_DSI_D3p	O, Analog	MIPI DSI Data Lane 3 positive.
AL20	MIPI_DSI_D3n	O, Analog	MIPI DSI Data Lane 3 negative.
AL14	MIPI_DSI_REXT	O, Analog	MIPI DSI reference resistor connection. Connect to VSS via a 200 Ohm resistor.

Table 25. SoC General Purpose I/O Interface

Pin Location(s)	Signal	Pin Type	Description
G12	GPIO_A[0]	I/O, CMOS	SoC GPIO[35], recommended for output only.
F10	GPIO_A[1]	I/O, CMOS	SoC GPIO[34], recommended for output only.
D6	GPIO_A[2]	I/O, CMOS	SoC GPIO[33], recommended for output only.

Table 26. HDMI CEC Interface

Pin Location(s)	Signal	Pin Type	Description
AE31	SM_HDMI_TX_CEC	I/Ood, CMOS	SM HDMI Consumer Electronics Control signal. This pin is 1.8V-only.

Table 27. HDMI HPD Interface

Pin Location(s)	Signal	Pin Type	Description
AE32	SM_HDMI_TX_HPD	I, CMOS	HDMI TX (source) hot plug detect. This pin is 1.8V-only.

Table 28. Two-Wire Serial SM Interface

Pin Location(s)	Signal	Pin Type	Description
AB31	SM_TW2_SCL	I/Ood, CMOS	SM TWSI2 serial clock.
AC31	SM_TW2_SDA	I/Ood, CMOS	SM TWSI2 serial data.
AH31	SM_TW3_SCL	I/Ood, CMOS	SM TWSI3 serial clock.
AJ31	SM_TW3_SDA	I/Ood, CMOS	SM TWSI3 serial data.

Table 29. SM Analog Interface

Pin Location(s)	Signal	Pin Type	Description
R27	SM_ADCI[0]	I, Analog	ADC input. Full input range 1.2V.
R28	SM_ADCI[1]	I, Analog	ADC input. Full input range 1.2V.
R32	SM_RCLKI	I, Analog	Oscillator/Crystal Input 25 MHz.
R31	SM_RCLKO	I/O, Analog	Crystal inverted output.

Table 30. System Manager (SM) Global Interface

Pin Location(s)	Signal	Pin Type	Description
AE29	SM_JTAG_SEL	Id, CMOS	SM JTAG port selection. 1 = Enable SM JTAG.
AD30	SM_POR_EN	Iu, CMOS	Enable on-chip power-on reset (POR_VDD) feature in SM.
AE30	SM_RSTIn	Iu, CMOS	SoC Active low reset input with internal pull-up.
AG31	SM_TCK	Id, CMOS	SM JTAG clock input.
AC26	SM_TDI	Iu, CMOS	SM JTAG SDATA IN.
AG29	SM_TDO	Ou, CMOS	SM JTAG SDATA OUT.
AE27	SM_TEST_EN	Id, CMOS	TEST enable. 1 = Enable SCAN. 0 = Enable ARM ICE JTAG connections.
AH32	SM_TMS	Iu, CMOS	SM JTAG Mode select signal (ARM or chip JTAG).
AG30	SM_TRSTn	Id, CMOS	SM JTAG reset.

Table 31. System Manager (SM) SPI Interface

Pin Location(s)	Signal	Pin Type	Description
AG25	SM_SPI2_SCLK	O, CMOS	SM SPI2 serial clock.
AL29	SM_SPI2_SDI	I, CMOS	SM SPI2 serial data input.
AM30	SM_SPI2_SDO	O, CMOS	SM SPI2 serial data output.
AJ30	SM_SPI2_SS0n	O, CMOS	SM SPI2 chip select 0.
AK31	SM_SPI2_SS1n	O, CMOS	SM SPI2 chip select 1.
AK32	SM_SPI2_SS2n	O, CMOS	SM SPI2 chip select 2.
AL30	SM_SPI2_SS3n	O, CMOS	SM SPI2 chip select 3.

Table 32. SM UART Interface

Pin Location(s)	Signal	Pin Type	Description
AK28	SM_URT0_RXD	I, CMOS	UART0 RX.
AL28	SM_URT0_TXD	O, CMOS	UART0 TX.
AD31	SM_URT1_RXD	I, CMOS	UART1 RX.
AC32	SM_URT1_TXD	O, CMOS	UART1 TX.

Table 33. SM FE Interface

Pin Location(s)	Signal	Pin Type	Description
U31	SM_FE_ATB_A	O, Analog	FE PHY Analog Test Port.
U32	SM_FE_ATB_B	O, Analog	FE PHY Analog Test Port.
AA31	SM_FE_RSET	I, Analog	FE PHY Calibration resistor. Connect a 6.04k ohm, ±1% resistor to VSS.
V30	SM_FE_RXn	I, Analog	FE PHY RX differential Input.
W30	SM_FE_RXp	I, Analog	FE PHY RX differential Input.
Y30	SM_FE_TXn	O, Analog	FE PHY TX differential output.
Y31	SM_FE_TXp	O, Analog	FE PHY TX differential output.

Table 34. Power – 1.8V

Pin Location(s)	Signal	Pin Type	Description
AG23	AVPLL_AVDD1P8	PWR	1.8V AVPLL analog power.
C8	CPUPLL_AVDD1P8	PWR	1.8V CPUPLL analog power.
E9	CPUTSEN_AVDD1P8	PWR	1.8V CPUTSEN analog power.
G20	EMMC_VDDIO1P8	PWR	1.8V EMMC power.
AG18	HDMI_TX_AVDD1P8	PWR	1.8V HDMI TX supply.
AJ13	KILOOTP_AVDD1P8	PWR	1.8V AVDD KILO OTP analog power.
E6	MEMPLL_AVDD1P8	PWR	1.8V memPLL analog power.
AH15	MIPI_DSI_AVDD1P8	PWR	1.8V MIPI DSI analog power.
AD9	M0_AVDD1P8	PWR	1.8V M0 analog power.
F30	PCIE_AVDD1P8	PWR	1.8V PCIe analog power.
K26	PCIE_PLL_AVDD1P8	PWR	1.8V PCIe PLL analog power.
C21	SDIO0_VDDIO1P8	PWR	1.8V SDIO analog power.
P29	SM_ADC_AVDD1P8	PWR	1.8V SM ADC analog power.
AA27	SM_FE_AVDD1P8	PWR	1.8V SM Ethernet PHY analog power.
U27	SM_OSC_VDDIO1P8	PWR	1.8V SM OSC analog power.
W27	SM_TSEN_AVDD1P8	PWR	1.8V SM TSEN analog power.
AJ27	SM_VDDIO1P8	PWR	1.8V SM digital I/O power.
E16	SYSPLL_AVDD1P8	PWR	1.8V SYSPLL analog power.
AJ15, C14, D12, N27	VDDIO1P8	PWR	1.8V SoC digital I/O power.

Table 35. Power – 3.3V

Pin Location(s)	Signal	Pin Type	Description
AA30	SM_FE_AVDD3P3	PWR	3.3V SM FE supply.
C26	USB2_AVDD3P3	PWR	3.3V USB2.0 analog power.
D23	USB2_VR_AVDD3P3	PWR	3.3V USB2.0 VR analog power.
D27	USB3_AVDD3P3	PWR	3.3V USB3.0 analog power.

Table 36. Power and Ground Pins (Sheet 1 of 3)

Pin Location(s)	Signal	Pin Type	Description
AF17	HDMI_TX_AVDD	PWR	HDMI TX analog power.
AG15	MIPI_DSI_AVDD	PWR	MIPI DSI analog power.
J28	PCIE_AVDD	PWR	PCIe analog power.
M29	PCIE_REFCLK_AVDD	PWR	PCIe REFCLK analog power.
F28	PCIE_TX_AVDD	PWR	PCIe TX analog power.
Y29	SM_FE_AVDD	PWR	SM Ethernet PHY analog power.
J26	PCIE_PLL_AVSS	GND	PCIe analog ground.
R26	SM_ADC_AVSS	GND	SM analog ground.
AA26	SM_FE_AVSS	GND	SM Ethernet PHY analog ground.
AC27	SM_VDD_CORE	PWR	SM digital core power.
F24	USB2_DVDD	PWR	USB 2.0 digital core power.
C29	USB3_AVDD	PWR	USB3.0 PHY analog power.
D29	USB3_DVDD	PWR	USB 3.0 PHY digital power.
AA16, AA20, AA24, AB10, AC14, AC18, AC22, AD16, AD18, AD20, AD24, M18, M20, N22, N24, P18, P20, T14, T20, T22, U16, U18, W16, W20, Y14, Y18, Y22	VDD_CORE	PWR	SoC core power.
AJ23	VDD_CORE_FB	PWR	Core voltage feedback compensation.
K14, K16, M14, M16, N16, P14, P16	VDD_CPU	PWR	SoC CPU power.
A4	VDD_CPU_FB	PWR	CPU voltage feedback compensation.
M9, M10, P9, P10, U9, W9	VDDQ	PWR	LPDDR4 I/O power 1.1V.
M12, N12, T12, V12, Y11, Y12	VDDQLP	PWR	LPDDR4 I/O power 1.1V or LPDDR4x I/O power 0.6V.

Table 36. Power and Ground Pins (Sheet 2 of 3)

Pin Location(s)	Signal	Pin Type	Description
A1, A2, A31, A32, AA2, AA9, AA12, AA14, AA18, AA22, AA29, AA32, AB4, AB7, AC16, AC20, AC24, AC29, AD3, AD6, AD7, AD10, AD12, AD14, AD22, AE26, AF3, AF7, AF11, AF15, AF16, AF19, AF21, AF23, AF25, AG13, AG27, AH6, AJ5, AJ11, AJ21, AJ25, AJ28, AK14, AK17, AK19, AK22, AK25, AL1, AL2, AL31, AL32, AM1, AM2, AM5, AM31, AM32, B1, B2, B4, B31, B32, C7, D5, D8, D14, D24, D26, F3, F6, F8, F12, F16, F20, F26, F32, G8, G10, G22, G24, G26, H3, H7, H28, J10, J12, J14, J16, J18, J20, J22, J24, J30, K3, K7, K10, K12, K18, K20, K22, K24, L1, L9, L10, L12, L20, L26, M4, M7, M22, M24, M28, N3, N13, N14, N18, N26, N29, P3, P12, P21, P22, P24, P32, R9, R10, R12, R30, T6, T16, T18, T24,	VSS	GND	Ground.

Table 36. Power and Ground Pins (Sheet 3 of 3)

Pin Location(s)	Signal	Pin Type	Description
U10, U14, U20, U22, U24, U26, U29, U30, V4, V11, W14, W18, W22, W24, W26, W29, Y3, Y6, Y16, Y20, Y24	VSS (continued...)	GND	Ground.

2. Pin Multiplexing

2.1. Pin Multiplexing Signal Descriptions

For complete pin multiplexing details, refer to Section 2.2., Pin Multiplexing Modes.

Note: The Pin Type in the tables in this section only represents the signal direction of the multiplexed signal. For other pin properties, such as open drain or pull-up, refer to the corresponding primary pin in the pin description table (see Section 1.2., Pin Descriptions).

Table 37. SoC Reset Strapping

Pin #	Pin Mux Name	Primary Pin Name	Pin Type	Description
AL10	boot_src[1]	SPDIFO	PU-boot	CPU Boot Source bit[1]
AF9	boot_src[0]	I2S2_MCLK	PD-boot	CPU boot source bit[0]. boot_src[1:0]: 00: ROM boot from SPI 01: Reserved 10: ROM boot from EMMC 11: Direct boot from SPI (Reserved for factory use only)
A13	software_strap[0] (USB_BOOTn)	SPI1_SDO	PU-boot	Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB 1: Boot from the device selected by boot_src
B10	software_strap[1]	SPI1_SS0n	PD-boot	Straps for software usage
AL13	legacy_boot	I2S1_DO[0]	PD-boot	Strap to reduce reset wait time 0: 2ms 1: 20ms
M31	software_strap[2]	SCRD0_RST	PD-boot	Straps for software usage
M32	software_strap[3]	SCRD0_DCLK	PD-boot	Straps for software usage
D6	cpuRstByps	GPIO_A[2]	PD-boot	CPU reset bypass strap 0: Enable reset logic inside CPU partition 1: Bypass reset logic inside CPU partition
F10	pllPwrDown	GPIO_A[1]	PD-boot	SYS/MEM/CPU PLL Power Down 1: Power Down 0: Power UP
G12	pllByps	GPIO_A[0]	PD-boot	SYS/MEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed

Table 37. SoC Reset Strapping (Continued)

Pin #	Pin Mux Name	Primary Pin Name	Pin Type	Description
AL28	SM_STRP[0]	SM_URT0_TXD	PD-boot	SM to SOC RSTn mode select 0: Releasing of the SoC reset does not wait for SM_PWR_OK (mode_0 of SM_SPI2_SS3n, system will assert this signal when SOC core power is ready). 1: Releasing of the SoC reset waits for SM_PWR_OK.
AM30	SM_STRP[1]	SM_SPI2_SDO	PD-boot	Software strap.
AJ30	SM_STRP[2]	SM_SPI2_SS0n	PD-boot	Software strap.
AK31	SM_STRP[3]	SM_SPI2_SS1n	PD-boot	Software strap.

Table 38. M0 Interface in LPDDR4 Mode (16-bit)

Pin Location(s)	Signal	Pin Type	Description
AC2	M0_LPDDR4_RSTn	O, HS_LVCMOS	M0 reset, active low.
M2	M0_LPDDR4_CKp	O, HS_LVCMOS	M0 clock positive.
L2	M0_LPDDR4_CKn	O, HS_LVCMOS	M0 clock negative.
R1	M0_LPDDR4_CKE	O, HS_LVCMOS	M0 clock enable.
P4	M0_LPDDR4_CSn	O, HS_LVCMOS	M0 chip select.
T3	M0_LPDDR4_A0	O, HS_LVCMOS	M0 LPDDR4 ADDR[0].
R2	M0_LPDDR4_A1	O, HS_LVCMOS	M0 LPDDR4 ADDR[1].
P6	M0_LPDDR4_A2	O, HS_LVCMOS	M0 LPDDR4 ADDR[2].
N1	M0_LPDDR4_A3	O, HS_LVCMOS	M0 LPDDR4 ADDR[3].
N4	M0_LPDDR4_A4	O, HS_LVCMOS	M0 LPDDR4 ADDR[4].
N2	M0_LPDDR4_A5	O, HS_LVCMOS	M0 LPDDR4 ADDR[5].
E1	M0_LPDDR4_DM0	O, HS_LVCMOS	M0 LPDDR4 Data mask BYTE[0].
J2	M0_LPDDR4_DM1	O, HS_LVCMOS	M0 LPDDR4 Data mask BYTE[1].
H6	M0_LPDDR4_DQ0	I/O, HS_LVCMOS	M0 LPDDR4 DQ[0].
C1	M0_LPDDR4_DQ1	I/O, HS_LVCMOS	M0 LPDDR4 DQ[1].
D4	M0_LPDDR4_DQ2	I/O, HS_LVCMOS	M0 LPDDR4 DQ[2].
F4	M0_LPDDR4_DQ3	I/O, HS_LVCMOS	M0 LPDDR4 DQ[3].
C2	M0_LPDDR4_DQ4	I/O, HS_LVCMOS	M0 LPDDR4 DQ[4].
H4	M0_LPDDR4_DQ5	I/O, HS_LVCMOS	M0 LPDDR4 DQ[5].
E2	M0_LPDDR4_DQ6	I/O, HS_LVCMOS	M0 LPDDR4 DQ[6].

Table 38. M0 Interface in LPDDR4 Mode (16-bit) (Continued)

Pin Location(s)	Signal	Pin Type	Description
D2	M0_LPDDR4_DQ7	I/O, HS_LVCMOS	M0 LPDDR4 DQ[7].
H1	M0_LPDDR4_DQ8	I/O, HS_LVCMOS	M0 LPDDR4 DQ[8].
K4	M0_LPDDR4_DQ9	I/O, HS_LVCMOS	M0 LPDDR4 DQ[9].
K2	M0_LPDDR4_DQ10	I/O, HS_LVCMOS	M0 LPDDR4 DQ[10].
K1	M0_LPDDR4_DQ11	I/O, HS_LVCMOS	M0 LPDDR4 DQ[11].
M6	M0_LPDDR4_DQ12	I/O, HS_LVCMOS	M0 LPDDR4 DQ[12].
L4	M0_LPDDR4_DQ13	I/O, HS_LVCMOS	M0 LPDDR4 DQ[13].
K6	M0_LPDDR4_DQ14	I/O, HS_LVCMOS	M0 LPDDR4 DQ[14].
F2	M0_LPDDR4_DQ15	I/O, HS_LVCMOS	M0 LPDDR4 DQ[15].
C3	M0_LPDDR4_DQS0p	I/O, HS_LVCMOS	M0 LPDDR4 DQSp BYTE 0.
H2	M0_LPDDR4_DQS1p	I/O, HS_LVCMOS	M0 LPDDR4 DQSp BYTE 1.
C4	M0_LPDDR4_DQS0n	I/O, HS_LVCMOS	M0 LPDDR4 DQSn BYTE 0.
G2	M0_LPDDR4_DQS1n	I/O, HS_LVCMOS	M0 LPDDR4 DQSn BYTE 1.

Table 39. M1 Interface in LPDDR4 Mode (16-bit)

Pin Location(s)	Signal	Pin Type	Description
Y1	M1_LPDDR4_CKp	O, HS_LVCMOS	M1 clock positive.
Y2	M1_LPDDR4_CKn	O, HS_LVCMOS	M1 clock negative.
V2	M1_LPDDR4_CKE	O, HS_LVCMOS	M1 clock enable.
T7	M1_LPDDR4_CSn	O, HS_LVCMOS	M1 chip select.
V3	M1_LPDDR4_A0	O, HS_LVCMOS	M1 LPDDR4 ADDR[0].
V1	M1_LPDDR4_A1	O, HS_LVCMOS	M1 LPDDR4 ADDR[1].
Y4	M1_LPDDR4_A2	O, HS_LVCMOS	M1 LPDDR4 ADDR[2].
W2	M1_LPDDR4_A3	O, HS_LVCMOS	M1 LPDDR4 ADDR[3].
AB2	M1_LPDDR4_A4	O, HS_LVCMOS	M1 LPDDR4 ADDR[4].
V6	M1_LPDDR4_A5	O, HS_LVCMOS	M1 LPDDR4 ADDR[5].
AH2	M1_LPDDR4_DM0	O, HS_LVCMOS	M1 LPDDR4 Data mask BYTE[0].
AF1	M1_LPDDR4_DM1	O, HS_LVCMOS	M1 LPDDR4 Data mask BYTE[1].
AL3	M1_LPDDR4_DQ0	I/O, HS_LVCMOS	M1 LPDDR4 DQ[0].
AL4	M1_LPDDR4_DQ1	I/O, HS_LVCMOS	M1 LPDDR4 DQ[1].
AF4	M1_LPDDR4_DQ2	I/O, HS_LVCMOS	M1 LPDDR4 DQ[2].
AH4	M1_LPDDR4_DQ3	I/O, HS_LVCMOS	M1 LPDDR4 DQ[3].
AF6	M1_LPDDR4_DQ4	I/O, HS_LVCMOS	M1 LPDDR4 DQ[4].

Table 39. M1 Interface in LPDDR4 Mode (16-bit) (Continued)

Pin Location(s)	Signal	Pin Type	Description
AJ2	M1_LPDDR4_DQ5	I/O, HS_LVCMOS	M1 LPDDR4 DQ[5].
AJ4	M1_LPDDR4_DQ6	I/O, HS_LVCMOS	M1 LPDDR4 DQ[6].
AM3	M1_LPDDR4_DQ7	I/O, HS_LVCMOS	M1 LPDDR4 DQ[7].
AF2	M1_LPDDR4_DQ8	I/O, HS_LVCMOS	M1 LPDDR4 DQ[8].
AE1	M1_LPDDR4_DQ9	I/O, HS_LVCMOS	M1 LPDDR4 DQ[9].
AB6	M1_LPDDR4_DQ10	I/O, HS_LVCMOS	M1 LPDDR4 DQ[10].
AB3	M1_LPDDR4_DQ11	I/O, HS_LVCMOS	M1 LPDDR4 DQ[11].
Y7	M1_LPDDR4_DQ12	I/O, HS_LVCMOS	M1 LPDDR4 DQ[12].
AD4	M1_LPDDR4_DQ13	I/O, HS_LVCMOS	M1 LPDDR4 DQ[13].
AH1	M1_LPDDR4_DQ14	I/O, HS_LVCMOS	M1 LPDDR4 DQ[14].
AG2	M1_LPDDR4_DQ15	I/O, HS_LVCMOS	M1 LPDDR4 DQ[15].
AK1	M1_LPDDR4_DQS0p	I/O, HS_LVCMOS	M1 LPDDR4 DQSp[0] BYTE 0.
AE2	M1_LPDDR4_DQS1p	I/O, HS_LVCMOS	M1 LPDDR4 DQSp[1] BYTE 1.
AK2	M1_LPDDR4_DQS0n	I/O, HS_LVCMOS	M1 LPDDR4 DQSn[0] BYTE 0.
AD2	M1_LPDDR4_DQS1n	I/O, HS_LVCMOS	M1 LPDDR4 DQSn[1] BYTE 1.

Table 40. General Purpose I/O Interface

Pin #	Pin Mux Name	Pin Type	Description
AG7	GPIO[0]	I/O, CMOS	General purpose I/O.
AJ7	GPIO[1]	I/O, CMOS	General purpose I/O.
AL5	GPIO[2]	I/O, CMOS	General purpose I/O.
AL6	GPIO[3]	I/O, CMOS	General purpose I/O.
AK10	GPIO[4]	I/O, CMOS	General purpose I/O.
AK7	GPIO[5]	I/O, CMOS	General purpose I/O.
AL7	GPIO[6]	I/O, CMOS	General purpose I/O.
AF9	GPIO[7][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
AG9	GPIO[8]	I/O, CMOS	General purpose I/O.
AM8	GPIO[9]	I/O, CMOS	General purpose I/O.
AK9	GPIO[10]	I/O, CMOS	General purpose I/O.
AJ9	GPIO[11]	I/O, CMOS	General purpose I/O.
AF13	GPIO[12]	I/O, CMOS	General purpose I/O.
AG11	GPIO[13]	I/O, CMOS	General purpose I/O.
AL10	GPIO[14][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
AK13	GPIO[15]	I/O, CMOS	General purpose I/O.

Table 40. General Purpose I/O Interface (Continued)

Pin #	Pin Mux Name	Pin Type	Description
AL11	GPIO[16]	I/O, CMOS	General purpose I/O.
AM13	GPIO[17]	I/O, CMOS	General purpose I/O.
AL8	GPIO[18]	I/O, CMOS	General purpose I/O.
AL13	GPIO[19][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
AM10	GPIO[20]	I/O, CMOS	General purpose I/O.
AK11	GPIO[21]	I/O, CMOS	General purpose I/O.
D6	GPIO[33][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
F10	GPIO[34][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
G12	GPIO[35][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
C11	GPIO[36]	I/O, CMOS	General purpose I/O.
C10	GPIO[37]	I/O, CMOS	General purpose I/O.
A8	GPIO[38]	I/O, CMOS	General purpose I/O.
B8	GPIO[39]	I/O, CMOS	General purpose I/O.
A6	GPIO[40]	I/O, CMOS	General purpose I/O.
B7	GPIO[41]	I/O, CMOS	General purpose I/O.
B6	GPIO[42]	I/O, CMOS	General purpose I/O.
B5	GPIO[43]	I/O, CMOS	General purpose I/O.
N31	GPIO[44]	I/O, CMOS	General purpose I/O.
P31	GPIO[45]	I/O, CMOS	General purpose I/O.
M32	GPIO[46][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
M31	GPIO[47][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
C15	GPIO[48]	I/O, CMOS	General purpose I/O.
A15	GPIO[49]	I/O, CMOS	General purpose I/O.
F14	GPIO[50]	I/O, CMOS	General purpose I/O.
G14	GPIO[51]	I/O, CMOS	General purpose I/O.
B15	GPIO[52]	I/O, CMOS	General purpose I/O.
B14	GPIO[53]	I/O, CMOS	General purpose I/O.
A13	GPIO[54][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
B12	GPIO[55]	I/O, CMOS	General purpose I/O.
B13	GPIO[56]	I/O, CMOS	General purpose I/O.
A10	GPIO[57]	I/O, CMOS	General purpose I/O.
B10	GPIO[58][1]	I/O, CMOS	General purpose I/O. Recommended as output only.
G16	GPIO[59]	I/O, CMOS	General purpose I/O.

1. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 41. SoC UART Interface

Pin #	Pin Mux Name[1]	Pin Type	Description
AL29	URT2A_CTSn	I, CMOS	UART2A CTSn.
AM30	URT2A_RTSn	O, CMOS	UART2A RTSn.
AL30	URT2A_RXD	I, CMOS	UART2A RXD.
AK32	URT2A_TXD	O, CMOS	UART2A TXD.
B7	URT2B_CTSn	I, CMOS	UART2B CTSn.
A6	URT2B_RTSn	O, CMOS	UART2B RTSn.
B5	URT2B_RXD	I, CMOS	UART2B RXD.
B6	URT2B_TXD	O, CMOS	UART2B TXD.

1. URT2A and URT2B are alternative pin locations for the same UART2 interface. UART2 function is not available when the VDD_CORE is powered off.

Table 42. Audio MIC PDM

Pin #	Pin Mux Name[1]	Pin Type	Description
AF13	PDMA_CLKIO	I/O, CMOS	PDM A Clock In/Out.
AG9	PDMA_DI[0]	I, CMOS	PDM A Data in.
AM8	PDMA_DI[1]	I, CMOS	PDM A Data in.
AF9	PDMB_CLKIO	I/O, CMOS	PDM B Clock In/Out.
AK10	PDMC_DI	I, CMOS	PDM C Data in.

1. PDMA, PDMB, and PDMC are alternative pin locations for the same PDM interface.

Table 43. PWM Alternate Interfaces

Pin #	Pin Mux Name	Pin Type	Description
AH32, AK11, AK32, B13, B8	PWM[0]	O, CMOS	Pulse-Width Modulation output data 0.
A10,A8, AC26, AL30, AM10	PWM[1]	O, CMOS	Pulse-Width Modulation output data 1.
AC32, AH31, AL11, C10	PWM[2]	O, CMOS	Pulse-Width Modulation output data 2.
AD31, AJ31, AK13, C11	PWM[3]	O, CMOS	Pulse-Width Modulation output data 3.

Table 44. Serial Transport Interface

Pin #	Pin Mux Name	Pin Type	Description
AM13	STS2_CLK	I, CMOS	Serial TS capture serial data clock.
AL11	STS2_SD	I, CMOS	Serial TS capture serial data.
AK13	STS2_VALD	I, CMOS	Serial TS capture valid flag.
AL8	STS2_SOP	I, CMOS	Serial TS capture start of packet.
AL6	STS3_CLK	I, CMOS	Serial TS capture serial data clock.
AL5	STS3_SD	I, CMOS	Serial TS capture serial data.
AG7	STS3_VALD	I, CMOS	Serial TS capture valid flag.
AJ7	STS3_SOP	I, CMOS	Serial TS capture start of packet.
AM8	STS4_CLK	I, CMOS	Serial TS capture serial data clock.
AG9	STS4_SD	I, CMOS	Serial TS capture serial data.
AK9	STS4_VALD	I, CMOS	Serial TS capture valid flag.
B6	STS5_CLK	I, CMOS	Serial TS capture serial data clock.
A6	STS5_SD	I, CMOS	Serial TS capture serial data.
A8	STS6_CLK	I, CMOS	Serial TS capture serial data clock.
C11	STS6_SD	I, CMOS	Serial TS capture serial data.
B13	STS7_CLK	I, CMOS	Serial TS capture serial data clock.
B12	STS7_SD	I, CMOS	Serial TS capture serial data.
A10	STS7_VALD	I, CMOS	Serial TS capture valid flag.

Table 45. SoC TWSI Interface

Pin #	Pin Mux Name[1]	Pin Type	Description
A15	TW1A_SCL	I/Ood, CMOS	TW1A serial clock.
C15	TW1A_SDA	I/Ood, CMOS	TW1A serial data.
B13	TW1B_SCL	I/Ood, CMOS	TW1B serial clock.
B12	TW1B_SDA	I/Ood, CMOS	TW1B serial data.

1. TW1A and TW1B are alternative pin locations for the same TWSI interface.

Table 46. Smart Card GPIO Interface

Pin #	Pin Mux Name	Pin Type	Description
B13	SCRD0_GPIO[0]	I/O, CMOS	Smart Card GPIO[0].
B12	SCRD0_GPIO[1]	I/O, CMOS	Smart Card GPIO[1].

Table 47. SM GPIOs

Pin #	Pin Mux Name	Pin Type	Description
AD31, AK32	CLK_25M	O, CMOS	25MHz digital clock output for system usage.
AB31	SM_GPIO[0]	I/O, CMOS	SM GPIO.
AC31	SM_GPIO[1]	I/O, CMOS	SM GPIO.
AE31	SM_GPIO[2]	I/O, CMOS	SM GPIO.
AE32	SM_GPIO[3]	I/O, CMOS	SM GPIO.
AD31	SM_GPIO[4]	I/O, CMOS	SM GPIO.
AC32	SM_GPIO[5]	I/O, CMOS	SM GPIO.
AG29	SM_GPIO[6]	I/O, CMOS	SM GPIO.
AC26	SM_GPIO[7]	I/O, CMOS	SM GPIO.
AH32	SM_GPIO[8]	I/O, CMOS	SM GPIO.
AH31	SM_GPIO[9]	I/O, CMOS	SM GPIO.
AJ31	SM_GPIO[10]	I/O, CMOS	SM GPIO.
AG25	SM_GPIO[11]	I/O, CMOS	SM GPIO.
AL29	SM_GPIO[12]	I/O, CMOS	SM GPIO.
AM30	SM_GPIO[13][1]	I/O, CMOS	SM GPIO. Recommended as output only.
AL30	SM_GPIO[14]	I/O, CMOS	SM GPIO.
AK32	SM_GPIO[15]	I/O, CMOS	SM GPIO.
AK31	SM_GPIO[16][1]	I/O, CMOS	SM GPIO. Recommended as output only.
AJ30	SM_GPIO[17][1]	I/O, CMOS	SM GPIO. Recommended as output only.
AK28	SM_GPIO[18]	I/O, CMOS	SM GPIO.
AL28	SM_GPIO[19][1]	I/O, CMOS	SM GPIO. Recommended as output only.

1. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 48. SM Peripherals

Pin #	Pin Mux Name	Pin Type	Description
AL30	SM_PWR_OK	I, CMOS	Power Good Detect input.
AC32, AK32	SM_TIMER[0]	O, CMOS	SM Timer output.
AD31, AL30	SM_TIMER[1]	O, CMOS	SM Timer output.
AL30	SM_URT1_CTSn	I, CMOS	SM UART1 CTSn.
AK31	SM_URT1_RTSn	O, CMOS	SM UART1 RTSn.
AG29	SM_FE_LED[0]	O, CMOS	FE PHY duplex/collision LED output
AC26	SM_FE_LED[1]	O, CMOS	FE PHY link speed LED output.
AH32	SM_FE_LED[2]	O, CMOS	FE PHY link/activity LED output.

Table 49. Test/Monitor Interfaces

Pin #	Pin Mux Name	Pin Type	Description
AL10	AVPLL_CLKO	O, CMOS	AVPLL monitor output.
B5	CPUPLL_CLKO	O, CMOS	CPU PLL monitor output.
B7	MEMPLL_CLKO	O, CMOS	MEM PLL monitor output.
AK32	MON_VDD1P8_OUT	O, CMOS	VDD1.8V monitor output.
AC32	PORB_AVDD_LV	O, CMOS	Power on reset for AVDD 1.8V power.
AJ30	PORB_AVDD33_LV	O, CMOS	Power on reset for AVDD 3.3V power.
AC32	POR_B_VOUT	O, CMOS	Combined power on reset for VDD, 1.8V, 3.3V power.
AD31	POR_VDDSOC_RSTB	O, CMOS	Power on reset for SoC VDD power.
B6	SYSPLL_CLKO	O, CMOS	SYS PLL monitor output.
AK31	VDD_CPU_PORB	O, CMOS	Power on reset for VDD CPU power.

Table 50. PHY Debug Interface

Pin #	Pin Mux Name	Pin Type	Description
B5	PHY_DBG[0]	O, CMOS	PHY Debug output data 0.
B6	PHY_DBG[1]	O, CMOS	PHY Debug output data 1.
B7	PHY_DBG[2]	O, CMOS	PHY Debug output data 2.
A6	PHY_DBG[3]	O, CMOS	PHY Debug output data 3.
B8	PHY_DBG[4]	O, CMOS	PHY Debug output data 4.
A8	PHY_DBG[5]	O, CMOS	PHY Debug output data 5.
C10	PHY_DBG[6]	O, CMOS	PHY Debug output data 6.
C11	PHY_DBG[7]	O, CMOS	PHY Debug output data 7.
M31	PHY_DBG[8]	O, CMOS	PHY Debug output data 8.
M32	PHY_DBG[9]	O, CMOS	PHY Debug output data 9.
G14	PHY_DBG[10]	O, CMOS	PHY Debug output data 10.
F14	PHY_DBG[11]	O, CMOS	PHY Debug output data 11.
B13	PHY_DBG[12]	O, CMOS	PHY Debug output data 12.
B12	PHY_DBG[13]	O, CMOS	PHY Debug output data 13.
A10	PHY_DBG[14]	O, CMOS	PHY Debug output data 14.
P31	PHY_DBG[15]	O, CMOS	PHY Debug output data 15.
B14	DBG_CLK	O, CMOS	Debug clock.

2.2. Pin Multiplexing Modes

This section describes the various modes related to the multiplexed pins. The primary pin name reflects the pinout name, while the Mode 0, Mode 1, ..., Mode 7 and Strap multiplex names are located in the respective columns.

Figure 2 shows the multiplexed pin naming scheme that is used for the SM Multiplexed pins.

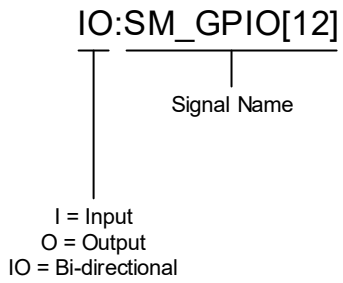


Figure 2. Example of the SM Multiplexed Pin Naming Scheme

Table 51. SM Group Multiplexing

Ball #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode Strap
AB31	SM_TW2_SCL	IO:SM_TW2_SCL	IO:SM_GPIO[0]	–	–	–	–	–	–	–
AC31	SM_TW2_SDA	IO:SM_TW2_SDA	IO:SM_GPIO[1]	–	–	–	–	–	–	–
AC32	SM_URT1_TXD	O:POR_B_VOUT	O:SM_URT1_TXD	IO:SM_GPIO[5]	O:PWM[2]	O:SM_TIMER[0]	O:PORB_AVDD_LV	–	–	–
AD31	SM_URT1_RXD	IO:SM_GPIO[4]	I:SM_URT1_RXD	O:CLK_25M	O:PWM[3]	O:SM_TIMER[1]	O:POR_VDDSOC_RSTB	–	–	–
AE32	SM_HDMI_TX_HPD	IO:SM_GPIO[3]	I:SM_HDMI_TX_HPD	–	–	–	–	–	–	–
AE31	SM_HDMI_TX_CEC	IO:SM_GPIO[2]	IO:SM_HDMI_TX_CEC	–	–	–	–	–	–	–
AH32	SM_TMS	I:SM_TMS	IO:SM_GPIO[8]	O:PWM[0]	O:SM_FE_LED[2]	–	–	–	–	–
AC26	SM_TDI	I:SM_TDI	IO:SM_GPIO[7]	O:PWM[1]	O:SM_FE_LED[1]	–	–	–	–	–
AG29	SM_TDO	O:SM_TDO	IO:SM_GPIO[6]	–	O:SM_FE_LED[0]	–	–	–	–	–
AH31	SM_TW3_SCL	IO:SM_GPIO[9]	IO:SM_TW3_SCL	O:PWM[2]	–	–	–	–	–	–
AJ31	SM_TW3_SDA	IO:SM_GPIO[10]	IO:SM_TW3_SDA	O:PWM[3]	–	–	–	O: SM_FE_AFE_ADC[0]	–	–
AJ30	SM_SPI2_SS0n	O:SM_SPI2_SS0n	IO:SM_GPIO[17] (Output Only)	–	–	–	–	O: SM_FE_AFE_ADC[1]	O:PORB_AVDD33_LV	SM_STRP[2]
AK31	SM_SPI2_SS1n	IO:SM_GPIO[16] (Output Only)	O:SM_SPI2_SS1n	–	–	–	–	O:SM_URT1_RTSn	O:VDD_CPU_PORB	SM_STRP[3]
AK32	SM_SPI2_SS2n	O:MON_VDD1P8_OUT	O:SM_SPI2_SS2n	IO:SM_GPIO[15]	O:PWM[0]	O:SM_TIMER[0]	O:URT2A_TXD	O: SM_FE_AFE_ADC[2]	O:CLK_25M	–
AL30	SM_SPI2_SS3n	I:SM_PWR_OK	O:SM_SPI2_SS3n	IO:SM_GPIO[14]	O:PWM[1]	O:SM_TIMER[1]	I:URT2A_RXD	O: SM_FE_AFE_ADC[3]	I:SM_URT1_CTSn	–
AM30	SM_SPI2_SDO	O:SM_SPI2_SDO	IO:SM_GPIO[13] (Output Only)	O:URT2A_RTSn	–	–	–	O: SM_FE_AFE_ADC[4]	–	SM_STRP[1]
AL29	SM_SPI2_SDI	I:SM_SPI2_SDI	IO:SM_GPIO[12]	I:URT2A_CTSn	–	–	–	O: SM_FE_AFE_ADC[5]	–	–
AG25	SM_SPI2_SCLK	O:SM_SPI2_SCLK	IO:SM_GPIO[11]	–	–	–	–	O: SM_FE_AFE_ADCCLK	–	–
AL28	SM_URT0_TXD	O:SM_URT0_TXD	IO:SM_GPIO[19] (Output Only)	–	–	–	–	–	–	SM_STRP[0]
AK28	SM_URT0_RXD	I:SM_URT0_RXD	IO:SM_GPIO[18]	–	–	–	–	–	–	–

1. Mode 0 is the default mode after reset. Strap mode is used only during power-up reset.

Figure 3 shows the multiplexed pin naming scheme that is used for the SoC Multiplexed pins.

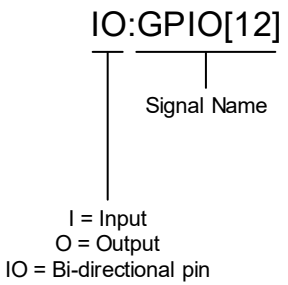


Figure 3. Example of the SoC Multiplexed Pin Naming Scheme

Table 52. SPI Interface Group Multiplexing

Ball #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode7	Mode Strap
A15	SDIO0_CDn	I:SDIO0_CDn	IO:GPIO[49]	IO:TW1A_SCL	—	—	—	—	—
C15	SDIO0_WP	I:SDIO0_WP	IO:GPIO[48]	IO:TW1A_SDA	—	—	—	—	—
B10	SPI1_SS0n	O:SPI1_SS0n	IO:GPIO[58](output only)	—	—	—	—	—	software_strap[1]
A10	SPI1_SS1n	IO:GPIO[57]	O:SPI1_SS1n	I:STS7_VALD	—	O:PWM[1]	—	O:PHY_DBG[14]	—
B13	SPI1_SS2n	IO:GPIO[56]	O:SPI1_SS2n	I:STS7_CLK	IO:TW1B_SCL	O:PWM[0]	IO:SCRD0_GPIO[0]	O:PHY_DBG[12]	—
B12	SPI1_SS3n	IO:GPIO[55]	O:SPI1_SS3n	I:STS7_SD	IO:TW1B_SDA	—	IO:SCRD0_GPIO[1]	O:PHY_DBG[13]	—
A13	SPI1_SDO	O:SPI1_SDO	IO:GPIO[54](output only)	—	—	—	—	—	software_strap[0]
B14	SPI1_SCLK	O:SPI1_SCLK	IO:GPIO[53]	—	—	—	—	O:DBG_CLK	—
B15	SPI1_SDI	I:SPI1_SDI	IO:GPIO[52]	—	—	—	—	—	—
G14	TW0_SCL	IO:GPIO[51]	IO:TW0_SCL	—	—	—	—	O:PHY_DBG[10]	—
F14	TW0_SDA	IO:GPIO[50]	IO:TW0_SDA	—	—	—	—	O:PHY_DBG[11]	—
G16	USB2_DRV_VBUS	O:USB2_DRV_VBUS	IO:GPIO[59]						

1. Mode 0 is the default mode after reset. Strap mode is used only during power-up reset.

Table 53. STSI Group Multiplexing

Ball #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	Mode Strap
B5	STS0_CLK	IO:GPIO[43]	I:STS0_CLK	O:CPUPLL_CLKO		I:URT2B_RXD	O:PHY_DBG[0]	—
B6	STS0_SOP	IO:GPIO[42]	I:STS0_SOP	O:SYSPLL_CLKO	I:STS5_CLK	O:URT2B_TXD	O:PHY_DBG[1]	—
B7	STS0_SD	IO:GPIO[41]	I:STS0_SD	O:MEMPLL_CLKO	—	I:URT2B_CTSn	O:PHY_DBG[2]	—
A6	STS0_VALD	IO:GPIO[40]	I:STS0_VALD	—	I:STS5_SD	O:URT2B_RTSn	O:PHY_DBG[3]	—
G12	GPIO_A[0]	IO:GPIO[35](output only)	—	—	—	—	—	pllByps
F10	GPIO_A[1]	IO:GPIO[34](output only)	—	—	—	—	—	pllPwrDown
D6	GPIO_A[2]	IO:GPIO[33](output only)	—	—	—	—	—	cpuRstByps
B8	STS1_CLK	IO:GPIO[39]	I:STS1_CLK	O:PWM[0]	—	—	O:PHY_DBG[4]	—
A8	STS1_SOP	IO:GPIO[38]	I:STS1_SOP	O:PWM[1]	I:STS6_CLK	—	O:PHY_DBG[5]	—
C10	STS1_SD	IO:GPIO[37]	I:STS1_SD	O:PWM[2]	—	—	O:PHY_DBG[6]	—
C11	STS1_VALD	IO:GPIO[36]	I:STS1_VALD	O:PWM[3]	I:STS6_SD	—	O:PHY_DBG[7]	—

1. Mode 0 is the default mode after reset.

Table 54. Smart Card Interface Group Multiplexing

Ball #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	Mode Strap
N31	SCRD0_CRD_PRES	I:SCRD0_CRD_PRES	IO:GPIO[44]	—	—	—	—	—
M31	SCRD0_RST	O:SCRD0_RST	IO:GPIO[47](output only)	—	—	—	O:PHY_DBG[8]	software_strap[2]
M32	SCRD0_DCLK	O:SCRD0_DCLK	IO:GPIO[46](output only)	—	—	—	O:PHY_DBG[9]	software_strap[3]
P31	SCRD0_DIO	IO:SCRD0_DIO	IO:GPIO[45]	—	—	—	O:PHY_DBG[15]	—

1. Mode 0 is the default mode after reset.

Table 55. AVIO_I2S Group Multiplexing

Ball #	Primary Pin Name	Mode 0[1]	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	Mode Strap
AL13	I2S1_DO[0]	IO:GPIO[19] (Output Only)	O:I2S1_DO[0]	—	—	—	O:AVIO_DBG[4]	legacy_boot
AM13	I2S1_DO[1]	IO:GPIO[17]	O:I2S1_DO[1]	—	I:STS2_CLK	—	O:AVIO_DBG[5]	—
AL11	I2S1_DO[2]	IO:GPIO[16]	O:I2S1_DO[2]	O:PWM[2]	I:STS2_SD	—	O:AVIO_DBG[6]	—
AK13	I2S1_DO[3]	IO:GPIO[15]	O:I2S1_DO[3]	O:PWM[3]	I:STS2_VALD	—	O:AVIO_DBG[7]	—
AK11	I2S1_LRCK	IO:GPIO[21]	IO:I2S1_LRCK	O:PWM[0]	O:ARC_TEST_OUT	—	O:AVIO_DBG[0]	—
AM10	I2S1_BCLK	IO:GPIO[20]	IO:I2S1_BCLK	O:PWM[1]	—	—	O:AVIO_DBG[1]	—
AL10	SPDIFO	IO:GPIO[14] (Output Only)	O:SPDIFO	—	—	O:AVPLL_CLKO	—	boot_src[1]
AK10	SPDIFI	IO:GPIO[4]	I:SPDIFI	I:PDMC_DI	—	—	—	—
AG11	I2S2_LRCK	IO:GPIO[13]	IO:I2S2_LRCK	—	—	—	—	—
AF13	I2S2_BCLK	IO:GPIO[12]	IO:I2S2_BCLK	IO:PDMA_CLKIO	—	—	—	—
AJ9	I2S2_DI[0]	IO:GPIO[11]	I:I2S2_DI[0]	—	—	—	—	—
AK9	I2S2_DI[1]	IO:GPIO[10]	I:I2S2_DI[1]	—	I:STS4_VALD	—	—	—
AM8	I2S2_DI[2]	IO:GPIO[9]	I:I2S2_DI[2]	I:PDMA_DI[1]	I:STS4_CLK	—	—	—
AG9	I2S2_DI[3]	IO:GPIO[8]	I:I2S2_DI[3]	I:PDMA_DI[0]	I:STS4_SD	—	—	—
AL8	I2S1_MCLK	IO:GPIO[18]	IO:I2S1_MCLK	—	I:STS2_SOP	—	O:AVIO_DBG[3]	—
AF9	I2S2_MCLK	IO:GPIO[7] (Output Only)	IO:I2S2_MCLK	IO:PDMB_CLKIO	—	—	—	boot_src[0]
AL7	HDMI_TX_EDDC_SCL	IO:HDMI_TX_EDDC_SCL	IO:GPIO[6]	—	—	—	—	—
AK7	HDMI_TX_EDDC_SDA	IO:HDMI_TX_EDDC_SDA	IO:GPIO[5]	—	—	—	—	—
AJ7	I2S3_DO	IO:GPIO[1]	O:I2S3_DO	—	I:STS3_SOP	—	O:AVIO_DBG[2]	—
AL6	I2S3_LRCK	IO:GPIO[3]	IO:I2S3_LRCK	—	I:STS3_CLK	—	—	—
AL5	I2S3_BCLK	IO:GPIO[2]	IO:I2S3_BCLK	—	I:STS3_SD	—	—	—
AG7	I2S3_DI	IO:GPIO[0]	I:I2S3_DI	—	I:STS3_VALD	—	—	—

1. Mode 0 is the default mode after reset. Strap mode is only used during power-up reset.

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Stresses above those listed in the Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 56. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VDDIO1P8	All IO supply voltage at 1.8V	-0.3	—	1.98	V
AVDD1P8	All Analog supply voltage at 1.8V	-0.3	—	1.98	
AVDD3P3	All analog supply voltage at 3.3V	-0.3	—	3.63	
AVDD	All analog supply voltage at 0.8V	-0.1	—	1.12	
DVDD	All digital supply voltage at 0.8V	-0.1	—	1.12	
SM_VDD_CORE	SM Core supply voltage	-0.1	—	0.96	
VDD_CPU	CPU supply Voltage	-0.1	—	1.12	
VDD_CORE	CORE supply voltage	-0.1	—	1.12	
M0_AVDD1P8	MEMPLL analog power at 1.8V	-0.3	—	1.98	
VDDQ	DDR4/LPDDR4 IO power	-0.3	—	1.32	
VDDQLP	DDR4/LPDDR4(x) IO power	-0.3	—	1.32	
V_{IN}	Input signal supplied by 3.3V SDIO_VDDIO3P3	-0.3	—	3.63	
V_{OUT}	Output signal supplied by 3.3V SDIO_VDDIO3P3	-0.3	—	3.63	
V_{PIN}	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	-0.3	—	1.98	
	Other signals supplied by VDDIO1P8	-0.3	—	1.98 or VDDIO1P8+0.2, whichever is lower	
$T_{STORAGE}$	Storage temperature	-55	—	+125[1]	°C

1. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.2. Recommended Operating Conditions

Table 57. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDDIO1P8	All IO supply voltage at 1.8V	—	1.71	1.8	1.89	V
AVDD1P8	All analog supply voltage at 1.8V	—	1.71	1.8	1.89	
AVDD3P3	All analog supply voltage at 3.3V	—	3.135	3.3	3.465	
AVDD	All analog supply voltage at 0.8V	Consumer	0.72	—	0.945	
		Industrial	0.72	—	0.984	
DVDD	All digital supply voltage at 0.8V	Consumer	0.72	—	0.945	
		Industrial	0.72	—	0.984	
SM_VDD_CORE	SM Core supply voltage	—	0.776	—	0.824	
VDD_CPU[1]	CPU supply voltage	Consumer	0.72	0.8	1.024	
		Industrial	0.72	—	1.050	
VDD_CORE[1]	CORE supply voltage	Consumer	0.72	0.8	0.945	
		Industrial	0.72	—	0.984	
VDD_CPU-VDD_CORE	Difference between CPU and CORE supplies[2]	—	-100	—	100	mV
M0_AVDD1P8	MEMPLL analog power at 1.8V	—	1.71	1.8	1.89	V
VDDQ, VDDQLP	IO power for DDR4	—	1.14	1.2	1.26	
	IO power for LPDDR4	—	1.06	1.1	1.17	
VDDQLP	IO power for LPDDR4x	—	0.57	0.6	0.65	
T_A	Ambient operating temperature[3]	Consumer	0	—	70	°C
		Industrial	-40	—	85	
T_J	Junction temperature	Consumer	0	—	105	
		Industrial	-40	—	125	
R_{M0_CAL}	DDR4/LPDDR4(x) PHY reference resistor, connect to VSS	—	—	120± 1%	—	Ohm
R_{USB2_REXT}	USB 2.0 PHY reference current resistor, connect to VSS	—	—	200± 1%	—	
$R_{USB2\_VBUS\_REXT}$	USB 2.0 PHY VBUS pin isolation resistor, connect to 5V VBUS voltage on USB link	—	—	30k± 1%	—	
R_{USB3_REXT}	USB 3.0 PHY reference current resistor, connect to VSS	—	—	200± 1%	—	
$R_{USB3\_VBUS\_REXT}$	USB 3.0 PHY VBUS pin isolation resistor, connect to 5V VBUS voltage on USB link	—	—	30k± 1%	—	
R_{PCIE_REXT}	PCIE PHY reference current resistor, connect to VSS	—	—	200± 1%	—	
$R_{HDMI\ TX\_REXT}$	HDMI TX reference current resistor, connect to VSS	—	—	1.62k ± 1%	—	
$R_{MIPI\ DSI\ REXT}$	MIPI DSI reference current resistor, connect to VSS	—	—	200 ± 1%	—	
$R_{SM\_FE\_REXT}$	Fast Ethernet PHY reference resistor, connect to VSS.	—	—	6.04k ± 1%	—	

1. The optimum core supply voltage is determined by the individual chip manufacturing process variation. The system software reads an index stored in the on-chip OTP memory and controls the VDD regulator output voltage. The nominal regulation of the VDD regulator should be within ±3%. For details refer to the *PV Compensation Application Note*.
2. For normal operation only, not applicable during power up/down.
3. The important parameter is maximum junction temperature. The maximum junction temperature needs to be observed in addition to the ambient temperature limits.

3.2.1. Power-up Sequence

Table 58. SL1640 Power-up Requirement

Power-up Timing Parameter	Power Rails	Min	Typ	Max	Units
Ramp rate	VDD_CORE, VDD_CPU	—	—	32	mV/uS
	All of DVDD	—	—	32	
	All of AVDD	—	—	32	
	All of VDDIO1P8	—	—	18	
	All of AVDD1P8	—	—	18	
	VDDQLP	—	—	18	
	VDDQ				
	M0_AVDD1P8				
	All AVDD3P3			100	
T1-T0	Time duration from SM_VDD_CORE/SM_FE_AVDD reached 0.8V to SOC_VDD_CORE ramp start	0	—	—	mS
T3-T2	Time duration between SOC_VDD_CORE reached 0.8V and All 1.8V power ramp start	0	—	—	
T5-T4	Time duration between SM_AVDD1P8/SM_VDDIO1P8 being stable to SM_FE_AVDD3P3 ramp start	0	—	—	

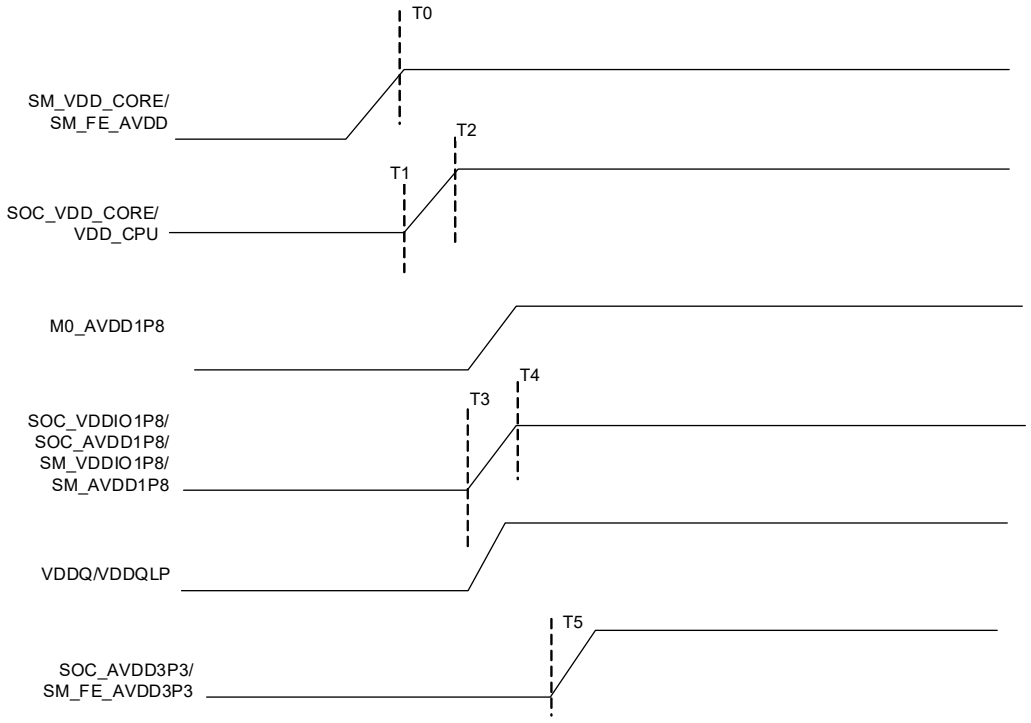


Figure 4. SL1640 Recommended power-up sequence in SoC and SM power domains

Note:

1. SOC_VDD_CORE starts ramping up (T1) after SM_VDD_CORE reaches its 100% of 0.8V (T0).
2. M0_AVDD1P8, VDDQ and VDDQLP shall follow the power sequence requirement from the DRAM devices if shared with the DRAM. Otherwise, no specific sequence is required between them or relative to other power rails.
3. VDD_CPU and SOC_VDD_CORE are recommended to ramp up relatively close to each other. No specific sequence is required between them.
4. SOC_VDDIO1P8/SOC_AVDD1P8/SM_VDDIO1P8/SM_AVDD1P8 starts ramping up (T3) after SOC_VDD_CORE reaches its 100% of 0.8V (T2).
5. SM_FE_AVDD3P3 starts ramping (T5) after the other SM/SOC rails have reached their thresholds (T4).

3.3. Crystal Specifications

Table 59. Crystal Specifications

Parameter	Condition	Typical	Unit
Fundamental Frequency	—	25	MHz
Frequency Tolerance	0 – 70 °C (for consumer) -40 - 85 °C (for industrial)	<= ± 50	ppm
Load Capacitance	—	8 [1]	pF
Max. ESR	—	60	ohm
Drive Level	—	35	uW
Mode of Oscillation	—	Fundamental	—

1. For more design details, please contact the Synaptics application engineering team.

3.4. Thermal Conditions for the SL1640 Device 458-pin BGA Package

Table 60. Thermal Conditions[1] for the SL1640 Device

Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
θ_{JA}	Thermal resistance-junction to ambient of the SL1640 device 458-pin BGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	18.85	—	°C/W
			Industrial	—	13.375	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	Consumer	—	14.37	—	
			Industrial	—	14.279	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	Consumer	—	13.12	—	
			Industrial	—	12.714	—	
Ψ_{JT}	Thermal characteristic parameter-junction to top center of the SL1640 device 458-pin BGA package $\Psi_{JT} = (T_J - T_{TOP})/P.$ T_{TOP} = Temperature on the top center of the package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	0.03	—	°C/W
			Industrial	—	0.0368	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	Consumer	—	0.06	—	
			Industrial	—	0.037	—	
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	Consumer	—	0.06	—	
			Industrial	—	0.037	—	
Ψ_{JB}	Thermal characteristic parameter-junction to top center of the SL1640 device 458-pin BGA package $\Psi_{JB} = (T_J - T_{BOARD})/P.$	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	—	—	°C/W
			Industrial	—	4.429	—	
θ_{JC}	Thermal resistance-junction to case of the SL1640 device 458-pin BGA package $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ P_{TOP} = Power Dissipation from the top of the package	JEDEC 4 in. x 4.5 in. 1-layer PCB with no air flow	Consumer	—	0.19	—	°C/W
			Industrial	—	0.149	—	

Table 60. Thermal Conditions[1] for the SL1640 Device (Continued)

Symbol	Parameter	Condition	Spec.	Min	Typ	Max	Units
θ_{JB}	Thermal resistance-junction to board of the SL1640 device 458-pin BGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow	Consumer	—	5.85	—	°C/W
			Industrial	—	4.577	—	

1. For definitions and usage of the thermal parameters in this table, refer to *JESD51-12.01*.

3.5. AC and DC Electrical Characteristics

3.5.1. Digital Pins Operating Conditions

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.

Table 61. Digital Operating Conditions (Sheet 1 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage with Schmitt Trigger disabled	All 1.8V Digital IO pins	—	0.65*VDDIO1P8	—	1.98	V
		HDMI_TX_HPD	—	2.0	—	5.3	
V_{IL}	Low level input voltage with Schmitt Trigger disabled	All 1.8V Digital IO pins	—	-0.3	—	0.35*VDDIO1P8	
		HDMI_TX_HPD	—	0	—	0.8	
V_{T+}	Low to High Threshold Point with Schmitt Trigger enabled	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	0.98	1.09	1.21	
		SDIO_DATA[3:0] SDIO_CMD EMMC_DATA[7:0] EMMC_CMD EMMC_STRB	—	1.07	—	—	
		SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn	—	0.95	1.06	1.16	
		Other 1.8V digital IO pins	—	1	1.12	1.23	

Table 61. Digital Operating Conditions (Sheet 2 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{T-}	High to Low Threshold Point with Schmitt Trigger enabled	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	0.76	0.86	0.97	V
		SDIO_DATA[3:0] SDIO_CMD EMMC_DATA[7:0] EMMC_CMD EMMC_STRB	—	—	—	0.68	
		SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn	—	0.68	0.76	0.85	
		Other 1.8V digital IO pins	—	0.67	0.76	0.84	

Table 61. Digital Operating Conditions (Sheet 3 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
R_{PU}	Pull-up Resistor	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TWO_SCL, TWO_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	32k	48k	79k	Ohm
		SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn	—	57k	87k	146k	
		Other 1.8V digital IO pins[1]	—	19k	26k	39k	
R_{PD}	Pull-down Resistor	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TWO_SCL, TWO_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	30k	44k	68k	
		SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn	—	54k	79k	127k	
		Other 1.8V digital IO pins[1]	—	18k	24k	34k	

Table 61. Digital Operating Conditions (Sheet 4 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{OL} @ 0.45V	DS[3:0]=0000	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URT0_TXD, SM_URT0_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	0.7	1.1	1.4	mA
	DS[3:0]=0001			1.1	1.6	2.1	
	DS[3:0]=0010			2.2	3.2	4.1	
	DS[3:0]=0011			3.3	4.8	6.2	
	DS[3:0]=0100			4.4	6.4	8.2	
	DS[3:0]=0101			5.5	7.9	10.2	
	DS[3:0]=0110			6.6	9.5	12.3	
	DS[3:0]=0111			7.7	11.1	14.3	
	DS[3:0]=1000			8.8	12.6	16.2	
	DS[3:0]=1001			9.8	14.2	18.3	
	DS[3:0]=1010			10.9	15.8	20.3	
	DS[3:0]=1011			12	17.4	22.3	
	DS[3:0]=1100			13.1	18.8	24.1	
	DS[3:0]=1101			14.2	20.4	26.1	
	DS[3:0]=1110			15.2	22	28.1	
	DS[3:0]=1111			16.3	23.5	30.1	
	DS[2:0]=000	Other 1.8V digital IO pins[1]	—	2.2	3.1	4.1	
	DS[2:0]=001			4.6	6.7	8.7	
	DS[2:0]=010			6.6	9.6	12.5	
	DS[2:0]=011			8.9	12.8	16.7	
	DS[2:0]=100			12.3	17.8	23.1	
	DS[2:0]=101			14.3	20.7	26.8	
	DS[2:0]=110			15.8	22.9	29.6	
	DS[2:0]=111			17.6	25.5	33	

Table 61. Digital Operating Conditions (Sheet 5 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{OH} @ VDDIO-0.45	DS[3:0]=0000	SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TWO_SCL, TWO_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA	—	0.7	1.1	1.5	mA
	DS[3:0]=0001			1.1	1.7	2.3	
	DS[3:0]=0010			2.2	3.3	4.5	
	DS[3:0]=0011			3.2	5.0	6.7	
	DS[3:0]=0100			4.3	6.6	8.9	
	DS[3:0]=0101			5.4	8.2	11.1	
	DS[3:0]=0110			6.4	9.8	13.2	
	DS[3:0]=0111			7.5	11.5	15.4	
	DS[3:0]=1000			8.5	13.0	17.4	
	DS[3:0]=1001			9.6	14.7	19.6	
	DS[3:0]=1010			10.6	16.3	21.8	
	DS[3:0]=1011			11.7	17.9	23.9	
	DS[3:0]=1100			12.7	19.4	25.9	
	DS[3:0]=1101			13.8	21.0	28.0	
	DS[3:0]=1110			14.8	22.6	30.0	
	DS[3:0]=1111			15.8	24.2	32.2	
I_{OH} @VDDIO-0.45V	DS[2:0]=000	Other 1.8V digital IO pins[1]	—	1.8	2.8	3.7	
	DS[2:0]=001			3.9	5.9	7.8	
	DS[2:0]=010			5.6	8.4	11.2	
	DS[2:0]=011			7.5	11.2	15.0	
	DS[2:0]=100			10.4	15.5	20.6	
	DS[2:0]=101			12.0	18.1	23.9	
	DS[2:0]=110			13.3	20.0	26.5	
	DS[2:0]=111			14.8	22.2	29.5	
Input Capacitance	—	—	—	—	—	3.2	pF

Table 61. Digital Operating Conditions (Sheet 6 of 6)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_I	Input Leakage Current	—	V_I=1.8V or 0V	—	—	±10	?A
I_{OZ}	Tri-state Output Leakage Current	—	V_O=1.8V or 0V	—	—	±10	

1. eMMC and SDIO pins are not included unless specified.

3.5.2. SD, SDIO Timing

3.5.2.1. SD, SDIO Default Mode Timing Parameters

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 62. SD, SDIO Default Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	25	25	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	—	—	10	
t_{THL}	Clock Fall time	—	—	—	10	
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	—	—	—	ns
t_{IH}	Input Hold time	—	—	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output delay time	Data Transfer Mode	0	—	14	ns
t_{ODLY}	Output delay time	Identification Mode	0	—	50	

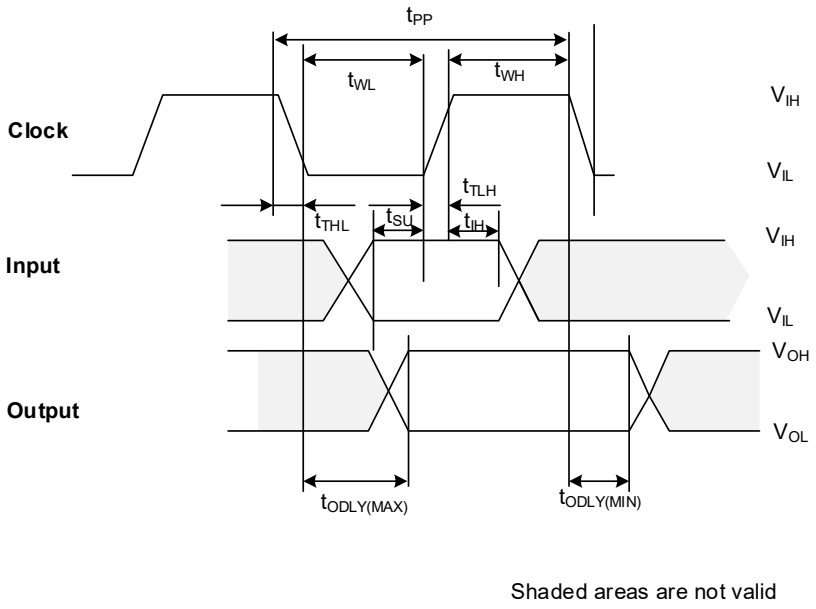


Figure 5. Timing Diagram Data Input/Output Referenced to Clock (Default)

3.5.2.2. SD, SDIO High-speed Mode Timing Parameters

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 63. SD, SDIO High-Speed Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	50	50	MHz
t_{WL}	Clock Low time	—	7	—	—	ns
t_{WH}	Clock High time	—	7	—	—	
t_{TLH}	Clock Rise time	—	—	—	3	
t_{THL}	Clock Fall time	—	—	—	3	
Inputs CMD, DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	—	—	—	ns
t_{IH}	Input Hold time	—	—	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer mode	0	—	14	ns
t_{OH}	Output Hold time	—	2.5	—	—	

3.5.2.3. SD, SDIO SDR104 Mode Timing Parameters

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 64. SD, SDIO SDR104 Mode Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode	—	0	208	208	MHz
t_{WL}	Clock Low time	—	1.44	—	—	ns
t_{WH}	Clock High time	—	1.44	—	—	
t_{TLH}	Clock Rise time	—	—	—	0.96	
t_{THL}	Clock Fall time	—	—	—	0.96	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	—	—	—	ns
t_{IH}	Input Hold time	—	—	—	—	

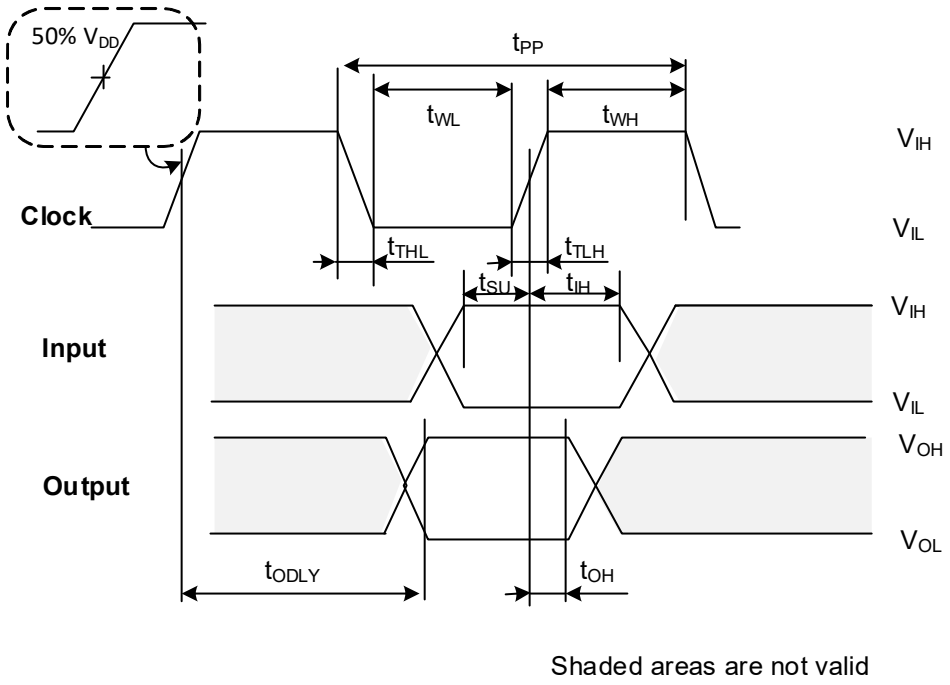


Figure 6. Timing Diagram Data Input/Output Referenced to Clock (High-speed & SDR104 mode)

3.5.3. Two-Wire Serial Interface (TWSI) Timing

3.5.3.1. TWSI Standard and Fast Mode Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 65. TWSI Standard and Fast Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SCL Clock Frequency	100 kHz	—	—	100	kHz
		400 kHz	—	—	400	
T_{TWSI_NS}	Noise Suppression Time at SCL, SDA Inputs	100 kHz	—	—	80	ns
		400 kHz	—	—	80	
T_{TWSI_R}	SCL, SDA Rise time	100 kHz	—	—	1000	
		400 kHz	—	—	300	
T_{TWSI_F}	SCL, SDA Fall Time	100 kHz	—	—	300	
		400 kHz	—	—	300	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000	—	—	
		400 kHz	600	—	—	
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz	4000	—	—	
		400 kHz	600	—	—	
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz	250	—	—	
		400 kHz	100	—	—	
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz	0	—	—	
		400 kHz	0	—	—	
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700	—	—	
		400 kHz	1300	—	—	
T_{TWSI_DLY}	SCL Low to SDA Data Out Valid	100 kHz	40	—	200	
		400 kHz	40	—	200	

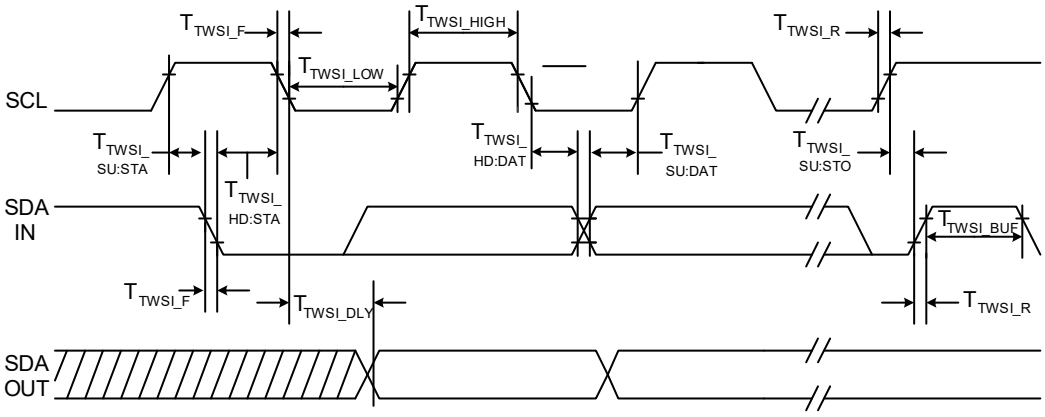


Figure 7. Two-Wire Serial Interface Timing

3.5.4. SPI Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 66. SCLK Cycle Time Configurable Range

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCLK}	SoC SPI SCLK cycle time	100 MHz SoC SPI controller input clock	20	—	655,340	ns
T_{SCLK}	SM SPI SCLK cycle time	25 MHz SM SPI controller input clock	80	—	2,621,360	

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 67. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	The first SPI cycle in a transfer	—	1.5	—	T_{SCLK}
		Subsequent SPI cycles	—	0.5	—	
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	Other than the last SPI cycle	—	0.5	—	
		The last SPI cycle in a transfer	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0.5	—	
		If Tx FIFO is empty	2	—	—	
T_{SET}	Setup time MISO with regard to SCLK active edge	—	13.8	—	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	0	—	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	T_{SCLK}
		Subsequent SPI cycles	—	0	—	

Table 67. Motorola SPI Mode 0/2 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	0.12	—	1.28	ns

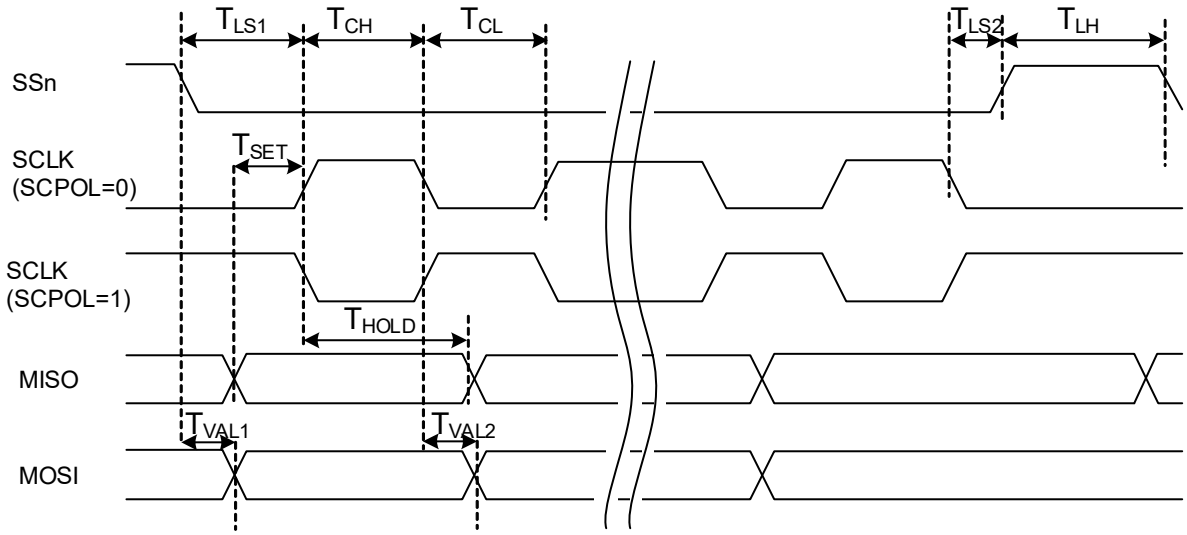


Figure 8. Motorola SPI Mode 0/2 (SCPH = 0)

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 68. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{LS1}	Time from SSn assertion to the first SCLK active edge	—	—	1.0	—	T_{SCLK}
T_{LS2}	Time from the last SCLK inactive edge to SSn de-assertion	—	—	1.0	—	
T_{CH}	SCLK high time	—	—	0.5	—	
T_{CL}	SCLK low time	—	—	0.5	—	
T_{LH}	SSn de-assertion Time between SPI cycles	If Tx FIFO is not empty at the end of the previous SPI cycle	—	0	—	
		If Tx FIFO is empty	1.5	—	—	

Table 68. Motorola SPI Mode 1/3 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SET}	Setup time MISO with regard to SCLK active edge	—	—	30	—	ns
T_{HOLD}	Hold time MISO with regard to SCLK active edge	—	—	30	—	
T_{VAL1}	Time from SSn assertion to MOSI MSB valid	The first SPI cycle in a transfer	—	1	—	T_{SCLK}
		Subsequent SPI cycles	—	0	—	
T_{VAL2}	Time from SCLK inactive edge to MOSI data valid	—	—	0.5	—	ns

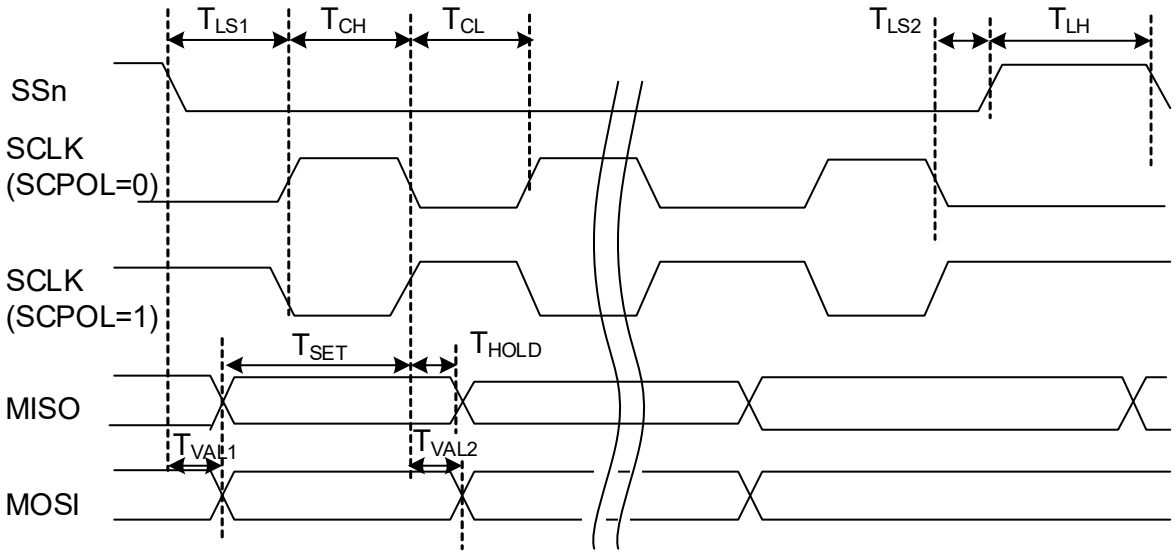


Figure 9. Motorola SPI Mode 1/3 (SCPH = 1)

3.5.5. UART Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 69. UART Timing

Symbol	Parameter	Condition	Min	**Typ**[1]	Max	Units
—	Tx bit width	±5%	—	8.68	—	µs
—	Rx bit width	±5%	—	8.68	—	

1. The typical values are for 115.2 kbaud. Other baud rates may apply.

3.5.6. JTAG Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 70. JTAG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CLK}	Clock cycle	—	—	200	—	ns
$T_{ISTRSTn}$	Set-up time for TRSTn	—	25%	—	—	T_{clk}
$T_{IHTRSTn}$	Hold time for TRSTn	—	0	—	—	ns
T_{ISTDI}	Set-up time for TDI	—	30%	—	—	T_{clk}
T_{IHTDI}	Hold time for TDI	—	0	—	—	ns
T_{OHTDO}	Hold time for TDO	—	0	—	—	ns
T_{OVTDO}	Data valid time for TDO	—	—	—	65%	T_{clk}
T_{RJT}	Rise time for all I/O	20-80%	10	—	—	ns
T_{FJT}	Fall time for all I/Os	80-20%	10	—	—	ns

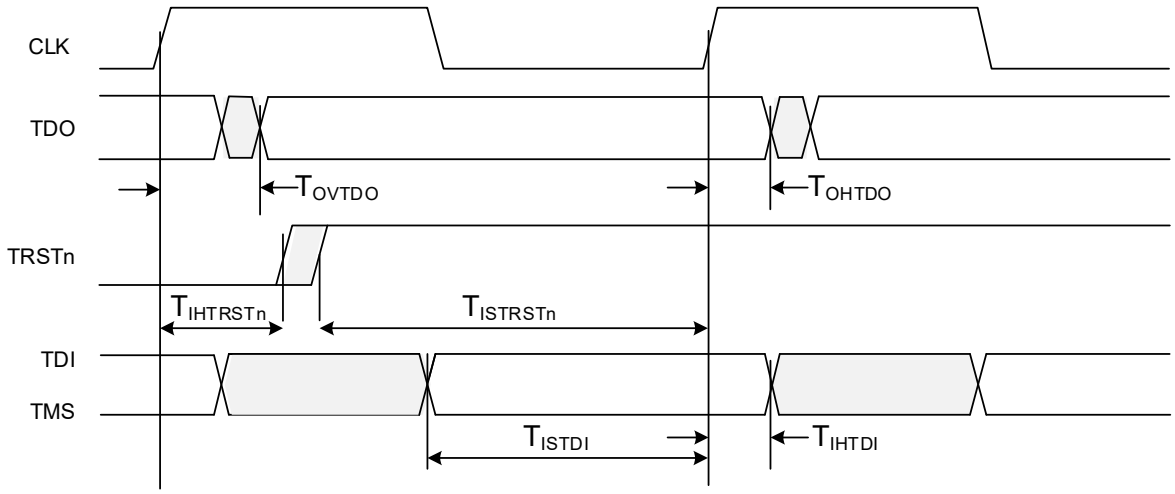


Figure 10. JTAG Timing

3.5.7. Transport Stream Serial Input Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 71. Transport Stream Serial Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{CLK}[1]	Input Clock Frequency	—	—	27	100	MHz
—	Clock Duty Cycle	—	30	50	70	%
T_{IS}	Transport Stream Serial Input set-up time for STS_DATA, STS_VALID, and STS_SOP	—	1	—	—	ns
T_{IH}	Transport Stream Serial Input hold time for STS_DATA, STS_VALID, and STS_SOP	—	1	—	—	

1. $f_{clk} = 1/t_{clk}$

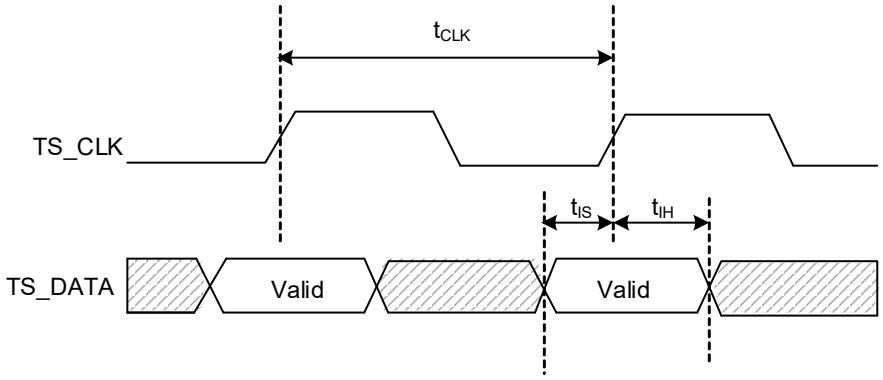


Figure 11. Transport Stream Serial Input Timing

3.5.8. I2S Timing

3.5.8.1. I2S Master Mode Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 72. I2S Master Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
F_S	—	—	32	—	192	KHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{SDPD}[1]	BCLK rising edge to SDATA output valid	—	—	$2T_{AIOSYSCLK}$	—	ns
T_{LRPD}	BCLK rising edge to LRCK valid	—	—	$2T_{AIOSYSCLK}$	—	
T_{SDS}	Set-up time SDATA input with regard to BCLK rising edge	—	—	$-3T_{AIOSYSCLK}$[2]	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK rising edge	—	—	$4T_{AIOSYSCLK}$[2]	—	
F_{MCLK}	MCLK (not shown) output frequency	—	6.144	24.576	49.152	MHz
D_{MCLK}	MCLK output duty cycle	—	—	50	—	%

1. BCLK may be inverted for more balanced setup and hold times.
2. Default AIOSYSCLK frequency is 200MHz.

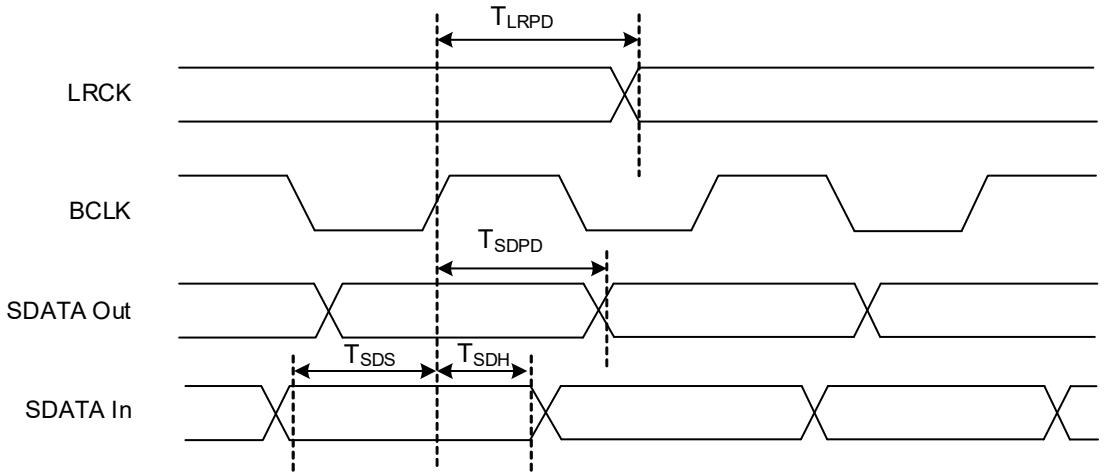


Figure 12. I2S Master Mode Timing

3.5.8.2. I2S Slave Mode Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 73. I2S Slave Mode Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	BCLK Frequency	—	16Fs	—	64Fs	Hz
F_{BCLK_PCM}	BCLK Frequency in PCM Mono mode	—	8Fs	—	256Fs	
F_{BCLK_TDM}	BCLK Frequency in TDM mode	—	16Fs	—	256Fs	
Fs	—	—	32	—	192	KHz
D_{BCLK}	BCLK duty cycle	—	—	50	—	%
T_{LRS}	Setup time LRCK input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK}$[1]	—	ns
T_{LRH}	Hold time LRCK input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK}$[1]	—	
T_{SDS}	Setup time SDATA Input with regard to BCLK active edge	—	—	$-3T_{AIOSYSCLK}$[1]	—	
T_{SDH}	Hold time SDATA Input with regard to BCLK active edge	—	—	$4T_{AIOSYSCLK}$[1]	—	
F_{MCLK}	MCLK (not shown) input frequency	—	—	24.576	49.152	MHz
D_{MCLK}	MCLK input duty cycle	—	—	50	—	%

1. Default AIOSYSCLK frequency is 200MHz.

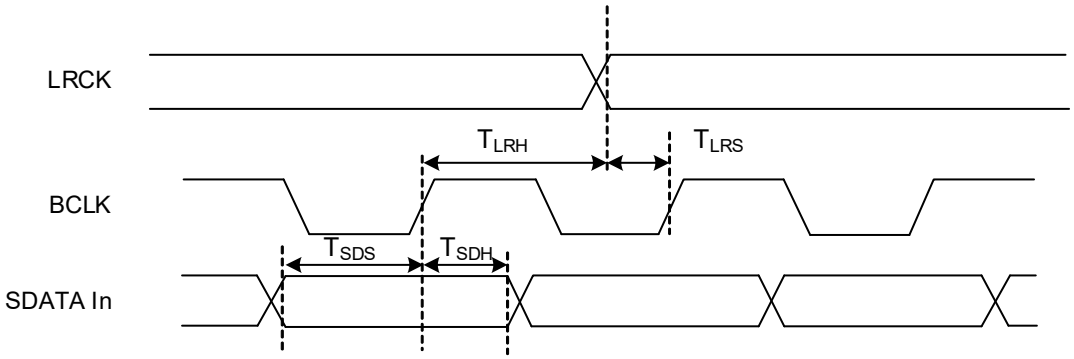


Figure 13. I2S Slave Mode Timing

3.5.9. Pulse-Width Modulation (PWM) Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 74. PWM Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PERIOD}	PWM	With 2-bit resolution	20ns	—	81.92µs	—
		With 16-bit resolution	655.35µs	—	2.684s	—
—	PWM Duty Cycle	—	0	—	100	%
—	PWM Duty Cycle Resolution	—	2	—	16	bit

3.5.10. ADC Inputs

3.5.10.1. ADC Electrical Information

(Over full range of values listed in the Table 57, Recommended Operating Conditions unless specified.)

Table 75. ADC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units
$T_{\_OUT}$	Digitalization Time	0.32	—	0.56	µs
V_{ADCIN_FS}	ADC_IN (analog input) full-scale voltage	—	—	1.2	V
—	Resolution	6	10	12	bits
INL	Integral Nonlinearity (INL), 10-bit mode	—	—	±2.2	LSB
DNL	Differential Nonlinearity (DNL), 10-bit mode	-0.97	—	1.9	LSB
OSE	Offset error	—	—	±0.7	%FS

3.5.11. USB 2.0 Timing

3.5.11.1. USB 2.0 DC Characteristics

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 76. USB 2.0 DC Electrical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	High (driven)	Note[1]	2.0	—	—	V
V_{IHZ}	High (floating)		2.7	—	3.6	
V_{IL}	Low		—	—	0.8	
V_{DI}	Differential Input Sensitivity	|(D+)-(D-)| Note[1]	0.2	—	—	
V_{CM}	Differential Common Mode Range	Includes VDI range Note[1]	0.8	—	2.5	
Input Levels for High-speed:						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	—	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	—	525	—	625	
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	—	-50	—	500	
Output Levels for Full-speed:						
V_{OL}	Low	Note[1], Note[2]	0.0	—	0.3	V
V_{OH}	High (Driven)	Note[1], Note[3]	2.8	—	3.6	
V_{OSE1}	SE1	—	0.8	—	—	
V_{CRS}	Output Signal Crossover voltage	Note[4]	1.3	—	2.0	
Output Levels for High-speed:						
V_{HSOI}	High-speed idle level	—	-10.0	—	10.0	mV
V_{HSOH}	High-speed data signaling high	—	360	—	440	
V_{HSOL}	High-speed data signaling low	—	-10.0	—	10.0	
V_{CHIRPJ}	Chirp J level (differential voltage)	—	700	—	1100	
V_{CHIRPK}	Chirp K level (differential voltage)	—	-900	—	-500	

Table 76. USB 2.0 DC Electrical (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input Capacitance for Full-speed:						
C_{IND}	Downstream Facing Port	Note[5]	—	—	150	pF
C_{INUB}	Upstream Facing Port (without cable)	Note[6]	—	—	100	
C_{EDGE}	Transceiver edge rate control capacitance	—	—	—	75	
Terminations:						
R_{PU}	Bus pull-up Resistor on Upstream facing port	1.5 kohm ±5%	1.425	—	1.575	kohm
R_{PD}	Bus pull-down Resistor on Downstream Facing Port	15 kohm ±5%	14.25	—	15.75	
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for full-speed)	—	300	—	—	
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	—	3.0	—	3.6	V
Termination in High-speed:						
V_{HSTERM}	Termination voltage in high-speed	—	-10	—	10	mV

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6V.
3. Measured with RL of 14.25 kohm to GND.
4. Excluding the first transition from the idle state.
5. Measured at A receptacle.
6. Measured at B receptacle.

3.5.11.2. USB 2.0 Source Electrical Characteristics

(Over full range of values listed in Table 57, Recommended Operating Conditions unless otherwise specified.)

Table 77. USB High-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics:						
T_{HSR}	Rise Time (10%–90%)	—	500	—	—	ps
T_{HSF}	Fall Time (10%–90%)	—	500	—	—	ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high speed termination)	—	40.5	—	49.5	ohm
Clock Timings:						
T_{HSDRAT}	High-speed Data Rate	—	479.760	—	480.240	Mbps
T_{HSFRAM}	Microframe Interval	—	124.9375	—	125.0625	ms

Table 77. USB High-speed Source Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{HSRFI}	Consecutive Microframe Interval Difference	—	—	—	4 high-speed bit times	—

Table 78. USB Full-speed Source Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Driver Characteristics:						
T_{FR}	Rise Time	—	4	—	20	ns
T_{FF}	Fall Time	—	4	—	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF} Note[1]	90	—	111.11	%
Z_{DRV}	Driver Output Resistance for driver which is not high-speed capable.	—	28	—	44	ohm
Clock Timings:						
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high speed capable.	Average bit rate	11.9940	—	12.0060	Mbps
T_{FDRATE}	Full-speed Data Rate for devices which are high-speed capable.	Average bit rate	11.9700	—	12.0300	Mbps
T_{FRAME}	Frame Interval	—	0.9995	—	1.0005	ms
T_{RFI}	Consecutive Frame Interval Jitter	No clock adjustment	—	—	42	ns
Full-speed Data Timings:						
T_{DJ1}	Source Jitter Total (including frequency tolerance): To Next Transition	Note[1] Note[2] Note[3] Note[4]	-3.5	—	3.5	ns
T_{DJ2}	For Paired transitions		-4	—	4	
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	Note[3]	-2	—	5	
T_{JR1}	Receiver jitter: To Next Transition	Note[3]	-18.5	—	18.5	
T_{JR2}	For Paired Transitions	—	-9	—	9	
T_{FEOPT}	Source SE0 interval of EOP	—	160	—	175	
T_{FEOPR}	Receiver SE0 interval of EOP	Note[5]	82	—	—	
T_{FST}	Width of SE0 interval during differential transition	—	—	—	14	

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

3.5.12. PCIe Timing

For electrical specifications (2.5 and 5.0GT/s), refer to PCI Express® Base Specification Revision 2.0.

3.5.13. HDMI TX

3.5.13.1. HDMI TX DC Operating Conditions

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 79. HDMI TX DC Operating Conditions for HDMI 1.4b

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OFF}	Single-ended standby (off) output voltage	—	AV_{cc}-10	—	AV_{cc}+10	mV
V_{SWING}	Single-ended output swing voltage	—	400	—	600	
V_H	Single-ended high level output voltage	If attached Sink supports only <=165 MHz	AV_{cc}-10	—	AV_{cc}+10	
		If attached Sink supports >165 MHz	AV_{cc}-200	—	AV_{cc}+10	
V_L	Single-ended low level output voltage	If attached Sink supports only <=165 MHz	AV_{cc}-600	—	AV_{cc}-400	
		If attached Sink supports >165 MHz	AV_{cc}-700	—	AV_{cc}-400	

Table 80. HDMI TX DC Characteristics for 3.4Gbps < R_{bit} ≤ 6.0Gbps at TP1

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{SWING}	Single-ended output swing voltage: Data channels 0, 1, 2	—	400	—	600	mV
	Single-ended output swing voltage: Clock channel	—	200	—	600	
V_H	Single-ended high level output voltage: Data channels 0, 1, 2	—	AV_{cc}-400	—	AV_{cc}+10	
	Single-ended high level output voltage: Clock channel	—	AV_{cc}-400	—	AV_{cc}+10	
V_L	Single-ended low level output voltage: Data channels 0, 1, 2	—	AV_{cc}-1000	—	AV_{cc}-400	
	Single-ended low level output voltage: Clock channel	—	AV_{cc}-1000	—	AV_{cc}-200	

3.5.13.2. HDMI TX AC Operating Conditions

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Table 81. HDMI TX AC Operating Conditions for 1.4b

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Rise time / fall time (20%-80%)	—	75	—	—	ps
—	Intra-Pair Skew at Source Connector	—	—	—	0.15	T_{bit}
—	Inter-Pair Skew at Source Connector	—	—	—	0.20	$T_{character}$
—	Clock duty cycle	—	40	50	60	%
—	TMDS Differential Clock Jitter	—	—	—	0.25	T_{bit}

Table 82. HDMI TX AC Characteristics for 3.4Gbps < R_{bit} ≤ 6.0Gbps at TP1

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Rise time / fall time (20%-80%): Data channels 0, 1, 2	—	42.5	—	—	ps
—	Rise time / fall time (20%-80%): Clock Channel	—	75	—	—	ps
—	Intra-Pair Skew at Source Connector	—	—	—	0.15	T_{bit}
—	Inter-Pair Skew at Source Connector	—	—	—	0.20	$T_{character}$
—	Clock duty cycle	—	40	50	60	%
—	TMDS Differential Clock Jitter	At TP2_EQ	—	—	0.30	T_{bit}

3.5.14. DDR4/LPDDR4 Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

Refer to JESD79-4C for DDR4 SDRAM specification.

Refer to JESD209-4A for LPDDR4 SDRAM specification.

3.5.15. eMMC Timing

(Over full range of values listed in Table 57, Recommended Operating Conditions unless specified.)

3.5.15.1. eMMC Timing - Default Bus

Table 83. eMMC Timing – Default Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode 3	—	0	—	26	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	10	—	—	ns
t_{WH}	Clock High time	—	10	—	—	
t_{TLH}	Clock Rise time	—	0.4	—	1.32	
t_{THL}	Clock Fall time	—	0.4	—	1.32	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	Note[1]	—	—	ns
t_{IH}	Input Hold time	—	Note[1]	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	—	Note[1]	—	—	ns

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications.

3.5.15.2. eMMC Timing - High-Speed Bus

Table 84. eMMC Timing – High-Speed Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency Data Transfer Mode 3	—	0	—	52	MHz
f_{OD}	Clock Frequency Identification Mode	—	0	—	400	kHz
t_{WL}	Clock Low time	—	—	—	—	ns
t_{WH}	Clock High time	—	—	—	—	
t_{TLH}	Clock Rise time	—	0.4	—	1.32	
t_{THL}	Clock Fall time	—	0.4	—	1.32	
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	Note[1]	—	—	ns
t_{IH}	Input Hold time	—	Note[1]	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Delay time	Data Transfer Mode	Note[1]	—	—	ns
t_{RISE}	Signal Rise time	—	0.4	—	1.32	
t_{FALL}	Signal Fall time	—	0.4	—	1.32	

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications.

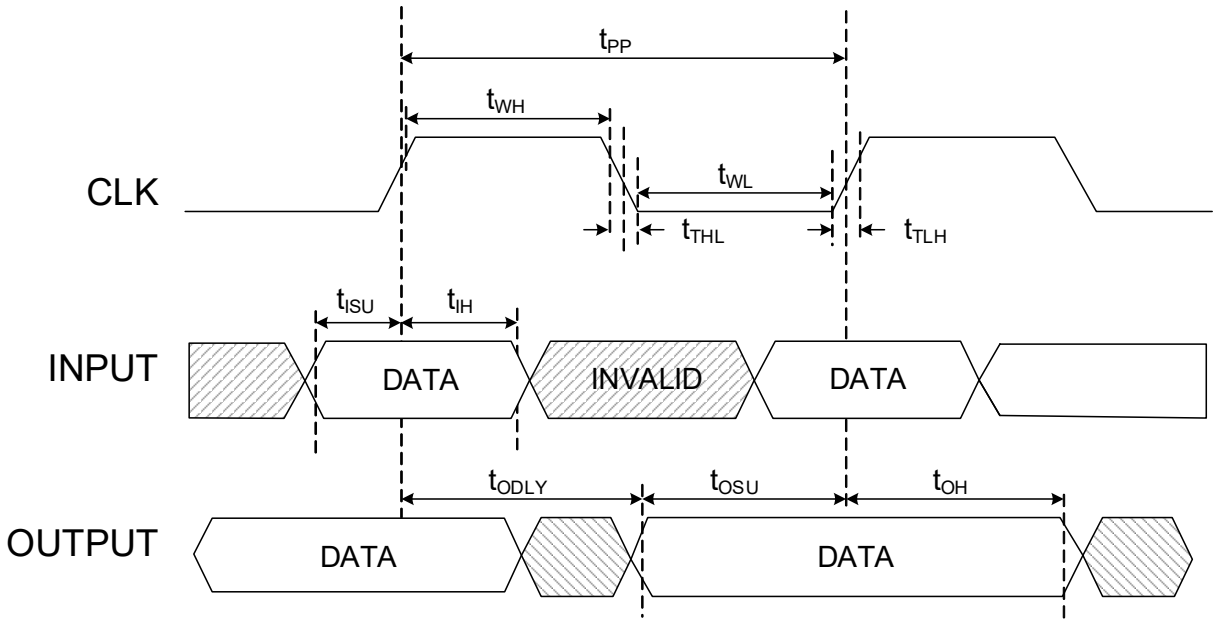


Figure 14. eMMC Timing - Default Bus and High-Speed Bus Interface Timing

3.5.15.3. eMMC Timing - High-Speed Dual Rate Bus

Table 85. eMMC Timing - High-Speed Dual Rate Bus

Symbol	Parameter	Condition	Min	Typ	Max	Units
—	Clock Frequency	—	45	—	55	MHz
Inputs DAT (referenced to Clock):						
t_{ISU}	Input Setup time	—	Note[1]	—	—	ns
t_{IH}	Input Hold time	—	Note[1]	—	—	
Outputs CMD, DAT (referenced to Clock):						
t_{ODLY}	Output Clock Delay	Data Transfer Mode	Note[1]	—	—	ns
t_{RISE}	Signal Rise Time	—	0.4	—	1.32	
t_{FALL}	Signal Fall Time	—	0.4	—	1.32	

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications

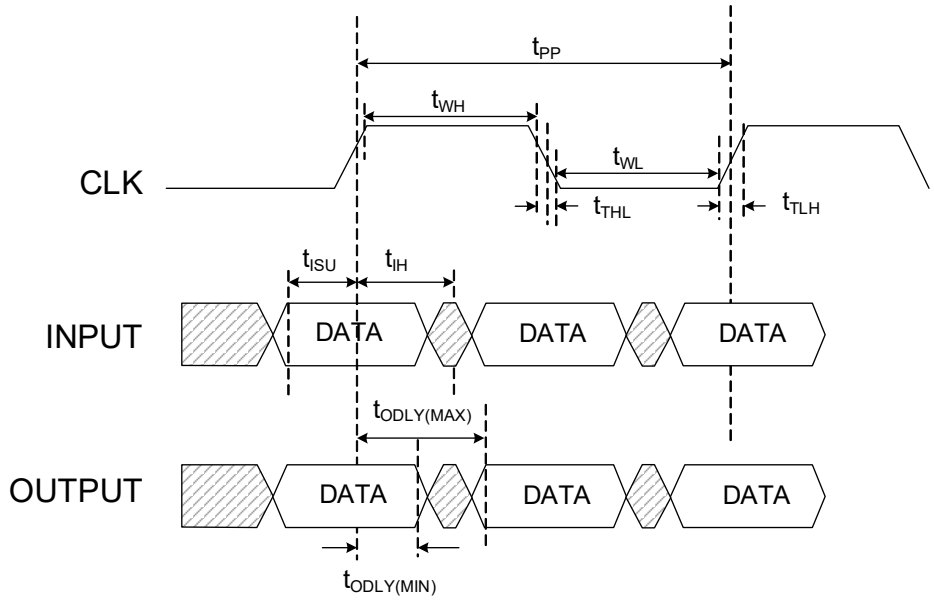


Figure 15. eMMC Timing - High-Speed Dual Rate Interface Timing

3.5.15.4. eMMC Timing - HS200 Mode & HS400 Mode

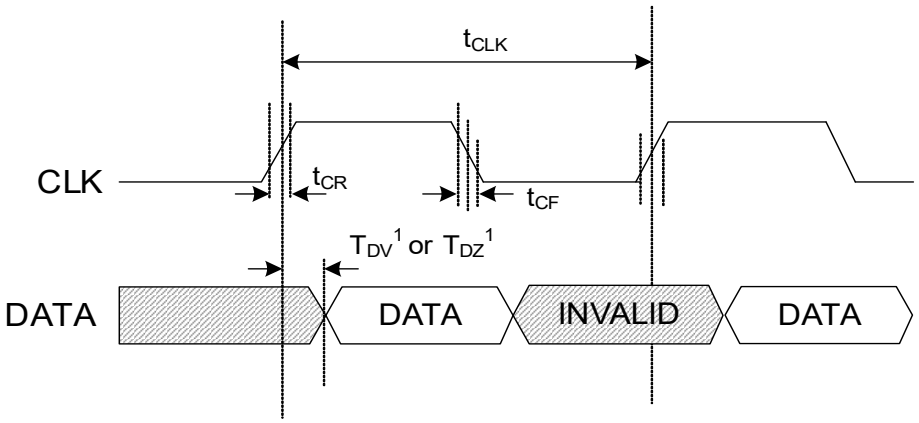
Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

3.5.16. Pulse Density Modulation

Table 86. Pulse Density Modulation (Classic PDM) Timing Parameters - SDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{CLK}[1]	PDM Clock Frequency	—	—	—	$F_{AIOSYSCLK}/4$[2]	MHz
t_D	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Input Clock Rise Time	10 - 90%	—	—	$T_{AIOSYSCLK}$[2]	ns
t_{CF}	Input Clock Fall Time	90 - 10%	—	—	$T_{AIOSYSCLK}$[2]	

1. $f_{CLK} = 1/t_{CLK}$
2. Default $F_{AIOSYSCLK}$ is 200MHz.



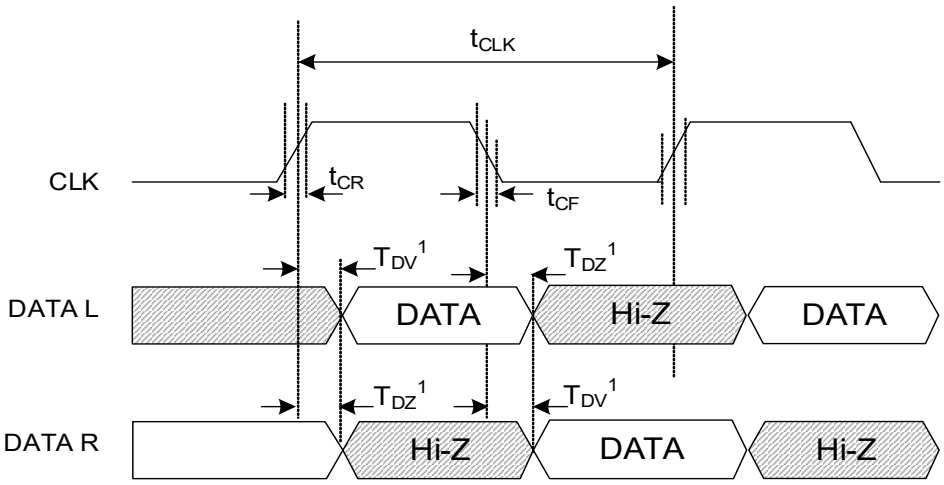
1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 16. PDM Timing - SDR Mode

Table 87. Pulse Density Modulation (Half Cycle PDM) Timing Parameters - DDR Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{CLK}[1]	PDM Clock Frequency	—	—	—	$F_{AIOSYSCLK}/4$[2]	MHz
t_D	Clock Duty Cycle	—	—	50	—	%
t_{CR}	Input Clock Rise Time	10 - 90%	—	—	$T_{AIOSYSCLK}$[2]	ns
t_{CF}	Input Clock Fall Time	90 - 10%	—	—	$T_{AIOSYSCLK}$[2]	ns

1. $f_{CLK} = 1/t_{CLK}$
2. Default $F_{AIOSYSCLK}$ is 200MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 17. PDM Timing - DDR Mode

3.5.17. MIPI DSI Characteristics

3.5.17.1. Input DC Specifications

Table 88 describes the Input DC Specifications.

Table 88. Input DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Apply to DATA0P/N Inputs:						
V_I	Input signal voltage range	—	-50	—	1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode	-10	—	10	µA
V_{GNDSH}	Ground shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Transient pin voltage level	—	-0.15	—	1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $V_{OH(absmax)}$	—	—	—	20	ns

3.5.17.2. MIPI DSI HS Line Drivers DC Specifications

Table 89. MIPI DSI HS Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 ? ≤ R_L ≤ 125 ?	140	200	270	mV
$?\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 ? ≤ R_L ≤ 125 ?	—	—	14	
V_{CMTX}	Steady-state common-mode output voltage	80 ? ≤ R_L ≤ 125 ?	150	200	250	
$?V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 ? ≤ R_L ≤ 125 ?	—	—	5	
V_{OHHS}	HS output high voltage	80 ? ≤ R_L ≤ 125 ?	—	—	360	
Z_{OS}	Single-ended output impedance	—	40	50	62.5	?
$?Z_{OS}$	Single-ended output impedance mismatch	—	—	—	10	%

3.5.17.3. MIPI DSI LP Line Drivers DC Specifications

Table 90. MIPI DSI LP Line Drivers DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output low-level SE voltage	—	-50	—	50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	—	110	—	—	?
$?Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$?Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%

3.5.17.4. MIPI DSI LP Line Receiver DC Specifications

Table 91. MIPI DSI LP Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input low voltage, not in ULPS	—	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULPS	—	—	—	300	
V_{IH}	Input high voltage	—	740	—	—	
V_{HYST}	Input hysteresis	—	25	—	—	

3.5.17.5. MIPI DSI Contention Line Receiver DC Specifications

Table 92. MIPI DSI Contention Line Receiver DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ILF}	Input low fault threshold	—	—	—	200	mV
V_{IHF}	Input high fault threshold	—	450	—	—	

3.5.17.6. MIPI DSI Clock Signal and Data-Clock Timing Specifications

Table 93. MIPI DSI Clock Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
—	Maximum Serial Data rate (forward direction)	80	—	2500	Mbps	Condition: On DATAP/N outputs. 80 ? ≤ R_L ≤ 125 ?
F_{DDRCLK}	DDR CLK frequency	40	—	1250	MHz	Condition: On CLKP/N outputs.
T_{DDRCLK}	DDR CLK period	0.8	—	25	ns	Condition: 80 ? ≤ R_L ≤ 125 ?
UI_{INST}	UI instantaneous	0.4	—	12.5	ns	The Max value corresponds to a minimum Mbps data rate.
?UI	UI variation	-10%	—	10%	UI	—
t_{CDC}	DDR CLK duty cycle	—	50	—	%	Condition: t_{CDC} = t_{CPH} / T_{DDRCLK}
t_{CPH}	DDR CLK high time	—	1	—	UI	—
t_{CPL}	DDR CLK low time	—	1	—	UI	—

3.5.17.7. MIPI DSI HS Line Drivers AC Specifications

Table 94. MIPI DSI HS Line Drivers AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_r	Differential output signal rise time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 ? For PHY operating at or below 1Gbps
		—	—	0.35	UI	For PHY operating above 1Gbps and below or at 1.5Gbps
		100	—	—	ps	For PHY operating below or at 1.5Gbps
t_f	Differential output signal fall time	—	—	0.30	UI	Condition: 20% to 80%, R_L = 50 ? For PHY operating at or below 1Gbps
		—	—	0.35	UI	For PHY operating above 1Gbps and below or at 1.5Gbps
		100	—	—	ps	For PHY operating below or at 1.5Gbps

3.5.17.8. MIPI DSI LP Line Driver and Receiver AC Specifications

For MIPI DSI LP line driver and receiver AC specifications, refer to the *MIPI D-PHY Specification v2*.

4. Mechanical Drawing

4.1. SL1640 Package Drawing

Note: The drawings in Figure 18, Figure 19, and Figure 20 are not to scale.

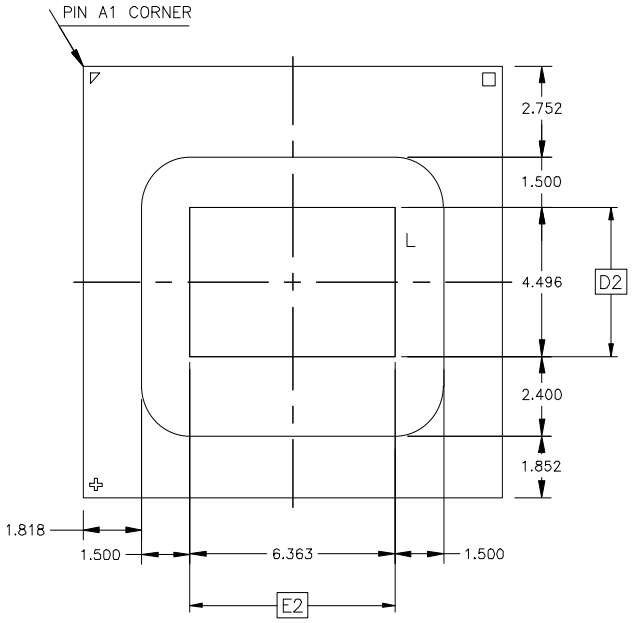


Figure 18. SL1640 Top View

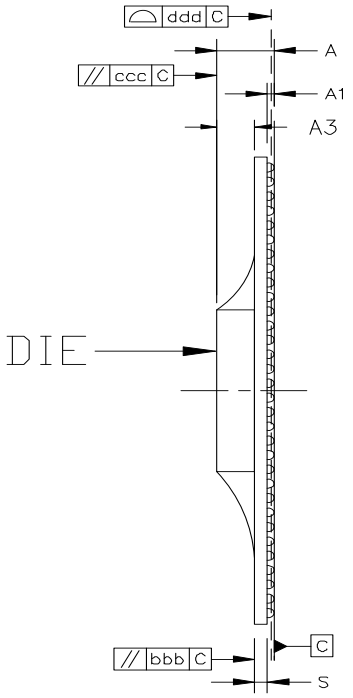


Figure 19. SL1640 Side View

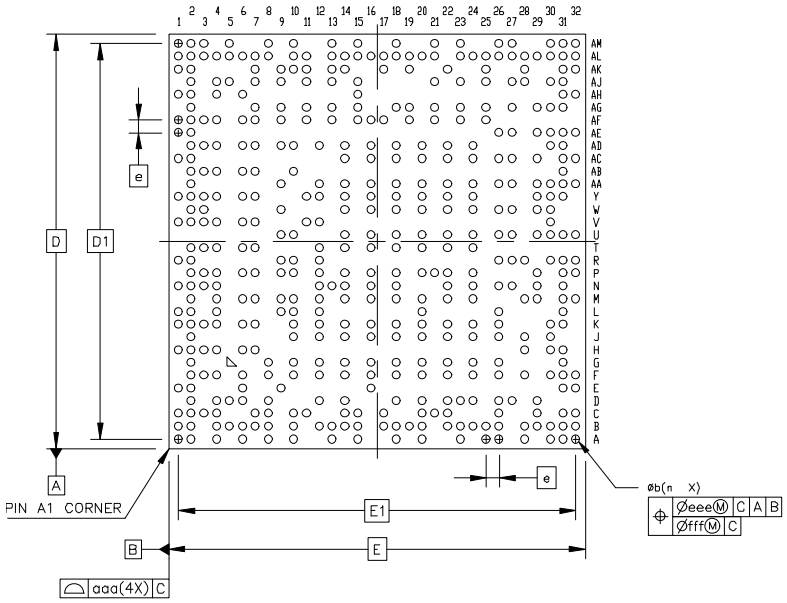


Figure 20. SL1640 Bottom View

Table 95. SL1640 Dimensions (in mm)

	Symbol	Common Dimensions		
		Min	Typ	Max
Total Thickness	A	1.230	1.330	1.430
Stand Off	A1	0.110	—	0.210
Substrate Thickness	S		0.300 REF	
Thickness from Substrate Surface to Die Backside	A3		0.870 REF	
Body Size	D		13.000 BSC	
	E		13.000 BSC	
Ball Diameter			0.250	
Ball Width	b	0.200	—	0.300
Ball Pitch	e		0.400 BSC	
Ball Count	n		458	
Edge Ball Center to Center	D1		12.4 BSC	
	E1		12.4 BSC	
Expose Die Size	D2		4.496 BSC	
	E2		6.363 BSC	
Package Edge Tolerance	aaa		0.100	
Substrate Parallelism	bbb		0.200	
Top Parallelism	ccc		0.200	
Coplanarity	ddd		0.080	
Ball Offset (Package)	eee		0.150	
Ball Offset (Ball)	fff		0.050	

5. Part Order Numbering / Package Marking

5.1. Part Order Numbering

Table 96 provides a list of the available options for ordering.

Table 96. SL1640 Part Order Options

Package Type	Part Number	Grade	Featured Option	Notes
458-pin FCBGA	SL1640A1-BYJXSZZ-T000-T	Consumer	Fully featured	Available now.
	SL1640A1-BYJXSYY-T000-T		HDMI disabled	
	SL1640A1-BYJXSZZ-H000-T	Industrial	Fully featured	Available in Q2 2025
	SL1640A1-BYJXSYY-H000-T		HDMI disabled	

5.2. Package Marking

Figure 21 shows a sample package marking and pin 1 location for the SL1640 device.

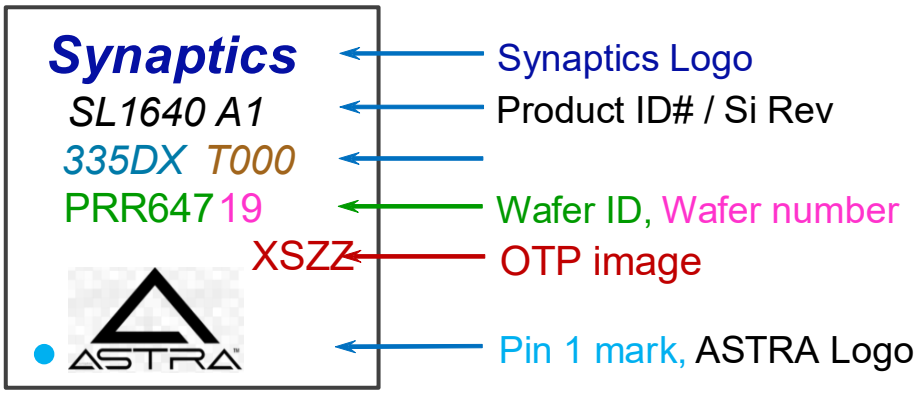


Figure 21. Package Marking and Pin 1 Location

6. References

- MIPI D-PHY Specification v2
- PV Compensation Application Note
- PCI Express® Base Specification Revision 2.0
- JESD209-4A Specification
- JESD51-12.01 Specification

7. Revision History

Last Modified	Revision	Description
March 2024	A	Release to production.
April 2024	B	Updated Section, Part Order Numbering, on page 93.
December 2024	C	Updated TBDs to actual values in Table 57, Recommended Operating Conditions, on page 47, and updated document to the latest SYNA template.
January 2025	D	Updated frequency “Up to 2.0 GHz” in Processors, on page 1. Updated industrial parts availability in Table 96, SL1640 Part Order Options, on page 93.

PN: 505-001415-01 Rev. D