Application Note

SL1640 General PCB Design and DDR4 & LPDDR4(x) Interface Layout Guidelines

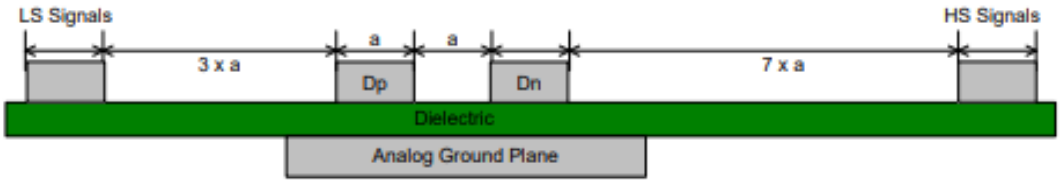
Abstract: This application note provides PCB design and layout guidelines for integrating DDR4 and LPDDR4(x) memory with the SL1640 processor. It outlines best practices for routing and signal integrity to ensure reliable system performance.

  | PN: 506-001529-01 Rev D

Contents

1. PCB Layout Guidelines

- Trace impedance of 100ohm differential (+/-10%) is required. For USB2.0, the trace impedance of 90ohm differential (+/-10%) is required.
- Matching to < 0.5mm (about 0.02 inch) between two different signals. Trace lengths should match by 0.25mm (about 0.01 inch) or less for differential pairs (same pair) of high-speed signals.
- The skew between any data lane and clock lane should be matched within +/-10ps on both package and PCB.
- Do not route trace over plane void or anti-pads. Return path should be VSS and continuous.
- Ensure ground return vias adjacent to the differential pair core vias to minimize crosstalk between lanes.
- Void the planes above the BGA pads to minimize the capacitive discontinuity.
- To minimize crosstalk, take care of signal traces which are routed close to the data differential pairs. The minimum recommended spacing is 3xa for low-speed non-periodic signals and 7xa for high-speed periodic signals. A continuous ground plane below the differential lines is required.



- TX and RX pairs should not be routed side-by-side in the same signal layer.
- Crosstalk should be accumulated total with all aggressors and meet the
- -30dB requirement until Nyquist frequency.
- The insertion loss of the trace is < 3dB (at Nyquist). For PCIE3.0, USB3.0 and Ethernet, the insertion loss of trace can be < 6dB. It should be monotonic, with no large insertion loss variations (+/-2dB) in the Nyquist frequency range. Trace should be shortest and low-loss as possible.

2. Power Supply Guidelines

- Supply bypass capacitors are recommended to minimize power supply noise. Noise analysis of the power delivery network is required to determine the actual values. Depending on their size, each capacitor will have a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that will determine the given capacitor's effectiveness over a frequency range. In general, several low-value capacitors (ceramic-type capacitors) should be placed as close as possible to the package pins. Larger-value capacitors (tantalum/electrolytic-type capacitors) can be placed farther away.
- The supply bypass capacitors should be connected as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane / trace as possible to reduce inductive and resistive losses. Typical capacitor placement can be under the package (other side of the board) or on the same side but close. An example of bypass capacitors is shown below.

Component	Value[1]
Power Supply Bypass Capacitors	0.01 µF, 0.1 µF, 4.7 µF, 10.0 µF

1. Smaller-value capacitors must be placed between the ferrite bead and the package.

- Both power plane and ground plane should be maintained continuously and have solid return path (not in bits and pieces). Pay attention to the void areas caused by vias. If the planes are cut down by vias, we need to compensate for the loss of the plane shape to make sure the effective width of the plane.

3. 4L non-HDI PCB Design Rules

3.1. NSMD Pad

- Minimum pin pitch = 0.4 mm (15.75 mil)
- Footprint pad / Paste mask of pad = 10mil (bga10)
- Solder mask of pad = 10 mil

3.2. SMD Pad

- Minimum pin pitch = 0.381 mm (15 mil)
- Footprint pad / Paste mask of pad = 12 mil (bga12)
- Solder mask of pad = 8 mil

3.3. Via

- Minimum through hole pad / Drill size = 14 / 8 mil

3.4. Spacing

- Minimum trace-to-trace = 3 mil
- Minimum trace-to-via = 3 mil
- Minimum trace-to-pad = 3 mil

The example stack-up/trace width and spacing of 4L non-HDI PCB is shown below.

Stack-up		Thickness(mil)			DK	Df	Material
	SM_TOP (0.5_PT_1OZ)	0.5			3.4		
L1			1.654	0.333oz +Plating			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L2			1.26	1oz			
	Core+PP (1.3mm)	51.18			4.6	0.018	S1000-2M
L3			1.26	1oz			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L4			1.654	0.333oz +Plating			
	SM_BOT (0.5_PT_1OZ)	0.5			3.4		
Thickness(mil):	63.988	63.988					
FinishPCBThinckness(mm):	1.6 (+/-0.16) mm						
PressPCBThinkness(mm):	1.48 (+/-0.08) mm						

Number	Type	Control Layer	Referance Layer	Adjust Line Width (mil)	Adjust Spacing (mil)	Adjust Line To Copper (mil)	Design Impedance (ohm)
1	Single-End	L1/L4	L2/L3	3.6			55.01
2	Single-End	L1/L4	L2/L3	4			52.93
3	Single-End	L1/L4	L2/L3	4.5			50.15
4	Differential	L1/L4	L2/L3	3.5	3		84.62
5	Differential	L1/L4	L2/L3	3.6	4		90.11
6	Differential	L1/L4	L2/L3	3.4	5.8		99.3
7	Differential	L1/L4	L2/L3	4	4		88.41

4. PCB Routing Rules for SL1640 DDR4 & LPDDR4(x) Interface

Note:

- This guideline recommends optimal layout practices for the DRAM section and is not a set of strict limitations.
- Synaptics reference layouts follow the guidelines, ensuring good operating timing margins.
- It is strongly recommended to copy DDR routing from the reference design.

4.1. General Rules

The general rules of usage are:

- All signals must be routed with a solid reference layer.
- Route single-end DQ[x] on the same layer within each BYTE group. If different layers are used, account for varying propagation delays during electrical length matching.
- Bit order can be scrambled within the same byte group for easier routing.
- Include via delay in length matching calculations.
- Place 1nF/10nF capacitors near each power pin of the SoC and all DRAMs for effective decoupling.
- Place 1nF/10nF capacitors at the edge of the power plane to reduce resonance.
- Place 1uF/10uF capacitors at the power rail input for both SoC and DRAM to avoid power trace bottlenecking.
- Place ground vias as close as possible to the cluster of signal vias.
- No more than two vias are recommended on any signal between the SoC and DRAMs, excluding low-speed DDR RSTn.

4.2. DDR4/LPDDR4(x) Package Trace Length Compensation

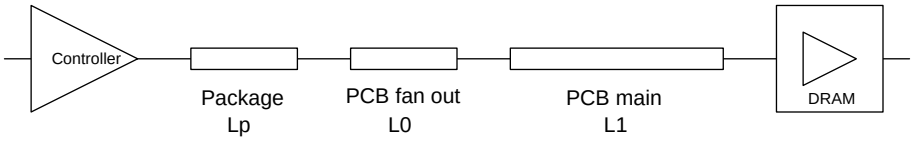
- Trace lengths between the chip die and package pins were not well matched due to package geometry, causing varying propagation delays and impacting timing margins. To compensate for this mismatch, proper PCB routing is essential. Refer to the table below for the electrical length of individual traces.
- Note that compensation should be made in addition to any special trace matching or tuning requirements mentioned in the sections that follow.
- The detailed constraint information can be found in the Synaptics reference layout files.

Byte Lane 0 Group			Byte Lane 1 Group		
Pin | Signal		Package Propagation Delay (ps)	Pin | Signal		Package Propagation Delay (ps)
AD2	M0_DQSn[0]	27.51	AK2	M0_DQSn[1]	34.40
AE2	M0_DQSp[0]	25.83	AK1	M0_DQSp[1]	34.00
AF1	M0_DM[0]	33.31	AH2	M0_DM[1]	30.20
AE1	M0_DQ[0]	29.26	AF6	M0_DQ[8]	17.43
AD4	M0_DQ[1]	20.35	AL3	M0_DQ[9]	33.76
Y7	M0_DQ[2]	12.27	AJ4	M0_DQ[10]	31.71
AG2	M0_DQ[3]	28.89	AJ2	M0_DQ[11]	29.45
AB3	M0_DQ[4]	19.21	AF4	M0_DQ[12]	24.08
AH1	M0_DQ[5]	31.88	AL4	M0_DQ[13]	32.80
AB6	M0_DQ[6]	16.80	AH4	M0_DQ[14]	25.96
AF2	M0_DQ[7]	35.03	AM3	M0_DQ[15]	41.52

Byte Lane 2 Group			Byte Lane 3 Group		
Pin | Signal		Package Propagation Delay (ps)	Pin | Signal		Package Propagation Delay (ps)
C4	M0_DQSn[2]	31.68	G2	M0_DQSn[3]	28.57
C3	M0_DQSp[2]	31.01	H2	M0_DQSp[3]	26.55
E1	M0_DM[2]	33.26	J2	M0_DM[3]	25.23
H6	M0_DQ[16]	16.69	K6	M0_DQ[24]	12.70
D2	M0_DQ[17]	28.71	H1	M0_DQ[25]	25.17
F4	M0_DQ[18]	25.52	L4	M0_DQ[26]	17.19
E2	M0_DQ[19]	29.74	K2	M0_DQ[27]	23.79
H4	M0_DQ[20]	19.48	K4	M0_DQ[28]	18.23
C2	M0_DQ[21]	34.52	K1	M0_DQ[29]	26.50
D4	M0_DQ[22]	25.73	M6	M0_DQ[30]	14.27
C1	M0_DQ[23]	34.33	F2	M0_DQ[31]	31.37

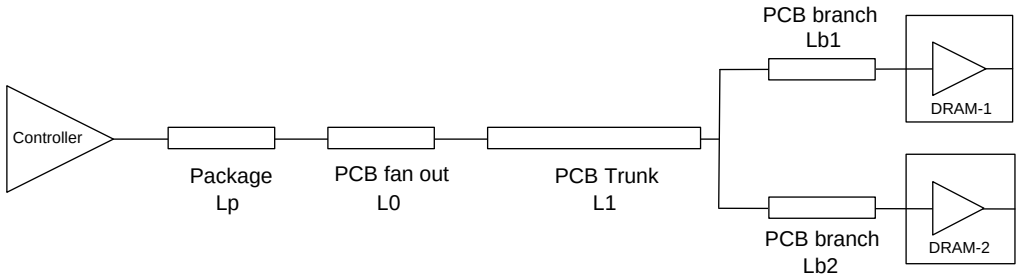
ADDRESS / COMMAND / CONTROL Group		
Pin | Signal		Package Propagation Delay (ps)
Y2	M0_CKn	25.62
Y1	M0_CKp	25.17
L2	M0_ACTn	24.99
M2	M0_RASn	23.35
Y4	M0_A[0]	19.53
N1	M0_A[1]	22.47
N4	M0_A[10]	16.66
V1	M0_A[2]	23.91
V6	M0_A[3]	15.27
P6	M0_A[4]	13.37
N2	M0_A[5]	21.46
R2	M0_A[6]	21.78
V3	M0_A[7]	19.83
T3	M0_A[8]	18.21
W2	M0_A[9]	21.70
AB2	M0_A[11]	25.50
W3	M0_A[12]	17.05
AC1	M0_A[13]	30.54
T4	M0_BA[0]	15.53
T7	M0_BA[1]	12.11
V2	M0_BG	22.93
V7	M0_CAL	11.59
T2	M0_CASn	21.96
R1	M0_CKE	21.92
P4	M0_CSn	18.03
P2	M0_WEn	22.02
P7	M0_ODT	9.52
AC2	M0_RSTN	25.53

4.3. DDR4 Data (DQ/DM/DQS) Bus



- All signals use point-to-point routing topology.
- Place the DRAM chip as close to the SoC chip as possible to minimize trace length.
- The impedance of single-ended signals should be targeted between 50 ohms and 55 ohms, with a tolerance of +/-10%.
- The impedance of differential pairs should be 85 ohms, with a tolerance of +/-10%.
- DQS must be routed in pairs on the same layer to match the propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- For each byte lane, the total signal trace length (Lp + L0 + L1) must be controlled within 70ps (or +/-70ps) of DQS.
- For each byte lane, the length matching for DQSp to DQSn (Lp + L0 + L1) should be controlled within 4.5ps (or +/- 4.5ps). Minimize the length gap between DQSp and DQSn as much as possible.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between DQSp / DQSn to other signals should be:
  - more than 1x the maximum of the intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum of the intra-pair air gap or trace width in the PCB main section (L1).

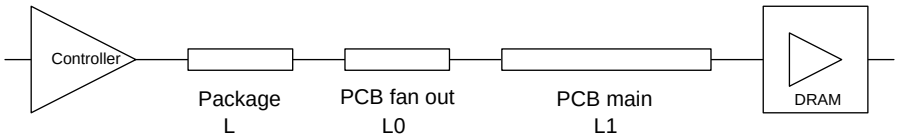
4.4. DDR4 CA Bus



- All signals use T-type routing topology.
- The impedance of single-ended signals for the branch segment (Lb*) should be 55 ohms, with a tolerance of +/-10%.
- The impedance of single-ended signals for the trunk segment (L1) should be 40 ohms, with a tolerance of +/-10%.
- The impedance of differential pairs for the branch segment (Lb*) should be 85 ohms, with a tolerance of +/-10%.
- The impedance of differential pairs for the branch segment (Lb*) should be 85 ohms, with a tolerance of +/-10%.
- The impedance of differential pairs for the trunk segment (L1) should be 65 ohms, with a tolerance of +/-10%.
- Place a 200-ohm shunt resistor across CLKp and CLKn at the end of each branch of CLK.
- For each CA channel, the total trace length of all CA/CS signals (Lp + L0 + L1 + Lb*) must be controlled within 100ps (or +/- 100ps) of CLK.
- For each CA channel, the length matching for CLKp to CLKn (Lp + L0 + L1 + Lb*) should be controlled within 0.5ps (or +/- 0.5ps).
- For each CA/CS/CLK signal, the length matching for Lb1 and Lb2 branches should be +/-1.6ps.
- For each channel, the total trace length of all DQS signals (Lp + L0 + L1 + Lb*) must be controlled within 150ps (or +/- 150ps) of CLK.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan-out section (L0).
  - more than 1.5x the trace width in the PCB trunk section (L1).
- The spacing (air gap between traces' edge) between CLKp / CLKn to other signals should be:
  - more than 1x the maximum of the intra-pair air gap or trace width in the PCB fan-out section (L0).
  - more than 3x the maximum of the intra-pair air gap or trace width in the PCB trunk section (L1).

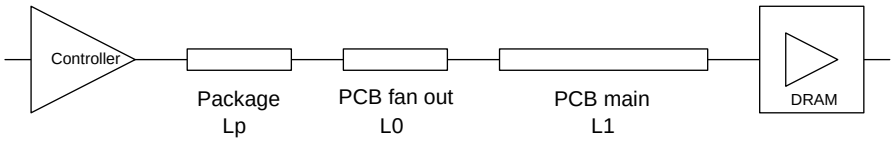
Note: Lb* represents Lb1 or Lb2.

4.5. LPDDR4(x) Data (DQ/DM/DQS) Bus



- All signals use point-to-point routing topology.
- Place the DRAM chip as close to the SoC chip as possible to minimize the trace length from SoC to DRAM.
- The impedance of single-ended signals should be 50 ohms +/- 10%. In the BGA break-out area, it may be 55 ohms +/- 10%.
- The impedance of differential pairs should be 85ohm +/- 10%.
- DQS must be routed in pairs on the same layer to match propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- For each byte lane, the length matching for DQ(DM) to DQ(DM) (Lp + L0 + L1) should be within +/-40ps.
- For each byte lane, the length matching for DQS to DQ(DM) (Lp + L0 + L1) should be within +/-40ps.
- For each byte lane, the length matching for DQSp to DQSn (Lp + L0 + L1) should be within +/-0.5ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan-out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between DQSp / DQSn to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

4.6. LPDDR4(x) CA Bus



- All signals use point-to-point routing topology.
- CLK must be routed in pairs on the same layer to match propagation delay and should use VSS instead of PWR as the reference plane for optimal current return.
- For each CA channel, the length matching for CA(CS) to CA(CS) (Lp + L0 + L1) should be +/- 65ps.
- For each CA channel, the length matching for CLK to CA(CS) (Lp + L0 + L1) should be +/- 65ps.
- For each CA channel, the length matching for CLKp to CLKn (Lp + L0 + L1) should be +/- 0.5ps.
- For each CA channel, the length matching for CLK to DQS (Lp + L0 + L1) should be +/-90ps.
- The spacing (air gap between traces' edge) between single-ended signals should be:
  - more than 1x the trace width in the PCB fan out section (L0).
  - more than 2x the trace width in the PCB main section (L1).
- The spacing (air gap between traces' edge) between CLKp / CLKn to other signals should be:
  - more than 1x the maximum intra-pair air gap or trace width in the PCB fan out section (L0).
  - more than 3x the maximum intra-pair air gap or trace width in the PCB main section (L1).

4.7. Board Stack-up

- The Synaptics EVK (Evaluation Kit) board uses the common 1.6mm PCB stack-up shown below.
- It is suggested that H34 (thickness between L3 and L4) be more than 5x the thickness of H12 (thickness between L1 and L2) to avoid cross talk between signals on L2 and L3.
- High-speed data signals that run on the top layer should reference L2 (VSS).
- Low-speed CA signals that run on the bottom layer should reference L3 (PWR).

Layer Name	Thickness	Dk @ 1GHz
Top SM	1.18 mil	3.8
Cu1	0.333oz + Planting	
Dielectric	3.2 mil	4.5
Cu2	1 oz	
Core	48.38	4.5
Cu3	1 oz	
Dielectric	3.2 mil	4.5
Cu4	0.333oz + Planting	
Bottom SM	1.18 mil	3.8

- The guaranteed signal quality was proven by simulation with the stack-up shown below. Contact Synaptics for the reference layout file.

Layer Name	Thickness	Dk @ 1GHz
Top SM	1.18 mil	3.8
Cu1	0.333oz + Planting	
Dielectric	3.2 mil	4.5
Cu2	1 oz	
Core	48.38	4.5
Cu3	1 oz	
Dielectric	3.2 mil	4.5
Cu4	0.333oz + Planting	
Bottom SM	1.18 mil	3.8

5. Revision History

Revision	Description
A	Initial release.
B	Added the following sections: • 1 PCB Layout Guidelines • 2 Power Supply Guidelines • 3 4L non-HDI PCB Design Rules
C	Minor update to document title.
D	Minor update to latest template.

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