

SL1680 Embedded IoT Processor

Electrical Specification Datasheet

PN: 505-001413-01 Rev D

Overview



The Synaptics SL-Series of embedded processors is a family of highly integrated AI-native Linux[®] and Android[™] SoCs optimized for multi-modal consumer, enterprise, and industrial IoT workloads with hardware accelerators for

edge inferencing, security, video, graphics, and audio.

The Synaptics SL1680 SoC incorporates multiple high-performance compute engines including a quad-core Arm[®]64 CPU subsystem, multi-TOPS NPU, GPU for advanced graphics and AI acceleration, and multimedia for image signal processing (ISP), 4K video encode/decode, and audio.

The SL1680 supports the Synaptics Astra IoT platform, delivering a unified experience through standards-based approaches, open software frameworks, full-featured AI toolkits, and market-ready evaluation systems.

In combination with Synaptics' best-in-class wireless connectivity portfolio, the SL1680 enables cost-optimized system solutions with performance-per-watt benefits for the IoT.

Features

CPU

- **Quad-Core Arm[®] Cortex[®]-A73 processor with Security Extensions**
- **Up to 2.1 GHz for each CPU, delivering up to 40000 DMIPS**
 - Support for power-gating individual cores and dynamic voltage and frequency scaling
- **Each processor has 64KB I-cache and 32KB D-Cache**
- **Each processor has dedicated Arm NEON[™] technology/VFPU**
 - 32 128-bit SIMD registers, crypto instructions
- **1 MB shared L2 Cache**

- **Arm CoreSight[™] technology-compatible debugging interface**
- **TrustZone[®] technology**
- **Supports standard tool chains (ARM, GNU)**

Memory Interface

- **DRAM controller**
 - 64-bit LPDDR4/LPDDR4x-3733
 - Supports optional 32-bit DDR configuration
 - Supports up to 4 GB memory space
 - Supports out-of-order issue of transactions to maximize DRAM utilization rate
 - Secure control
- **eMMC 5.1 Controller**
 - x1, x4 or x8-bit interface

Neural Processing Unit

- **Dedicated hardware for localized NN/machine learning applications**
 - Up to 7.9+ TOPS
- **Support for multiple DNN frameworks and optimized for TensorFlow[™] Lite inferencing via the SYNAP[™] toolkit**

Multi-Standard Video Decoding

- **Video decoding**
 - AV1 Main Profile (8- or 10-bit, YUV 4:2:0) 2160p60
 - H.265 main 8-bit and 10-bit (ITU-R BT.2020)
 - VP9 Profiles 0 and 2 (8- or 10-bit, YUV 4:2:2)
 - H.264 Baseline, Main and High Profiles; MVC (Multiview Video Coding)
 - MPEG-2 Simple and Main Profiles
 - VP8
- **Flexible support for PIP (2160p60/2160p60) and Multi-View (1 x 2160p60 and 3 x 1080p60)**
- **Support for single-stream 2160p H.265/VP9 decode that can reach up to 90-100 fps**
- **Support for up to 1080p120 single-stream decode**
- **Still Picture - H.264, MPEG2 I picture decode**

Multi-Standard Video Encoding/ Transcoding

- **Support for up to two streams encoding:**
 - 1080p60: H.264 or VP8 (per stream)
- **Support for simultaneous 2160p60 decode and 1080p60 transcode**

Audio Decoding/Processing

- **Far-Field Voice (FFV) & Keyword Detection**
- **Microphone(s) input processing supported**
- **Audio decompression of various formats supported**
- **Audio post-processing**

2D & 3D Graphics

- **GPU based graphics engine (Imagination™ PowerVR™ Series9XE GE9920)**
 - HDR-enabled
 - Geometry shader and Tessellation shader included
 - Support for OpenGL® ES™ 1.1/2.0/3.0/3.1/3.2/ DirectFB/OpenCL™ 1.2 / Vulkan® 1.1
 - Support for Android Extension Pack
 - Up to 3840x2160 resolution
 - 3D capable
 - 5.6 G pixels/s
 - 200 M polygons/s
 - 89.6 16-bit GFLOPS, 44.8 32-bit GFLOPS

Video/Graphics Display Pipeline with QDEO™

- **Two independent display output paths:**
 - Display path #1:
 - Output after MP/GFX0(or PIP)/GFX1 overlay
 - Output through HDMI Tx (up to 2160p60) / DSI (up to 2160p30)
 - Supports gamma correction and low-latency mode (for both source/sink devices)
 - Display path #2:
 - Output from GFX0(or PIP)/GFX1/GFX2 selection
 - 1080p60 output through DSI only
 - Supports gamma correction
- **MP:**
 - Any conversion between SDR and HDR (HDR10, HLG)
 - Scaling up and scaling down
 - Detail and edge enhancement
 - Flesh tone detection

- Luma and Chroma transition improvement
- Adaptive contrast enhancement
- Intelligent color re-mapper (chroma enhancement)
- 90/180/270 rotation
- Horizontal and vertical flip
- Compression artifact reduction
- Local dimming
- Gamma correction
- **GFX0 (or PIP) / GFX1:**
 - Scaling up only
 - Any conversion between SDR and HDR (HDR10, HLG)
- **GFX2:**
 - Scaling up only
 - Offline video pipeline (OVP):
 - Offline deinterlacer
 - Offline scalar (up and down)

Security

- **250MHz Secure CPU (Arm Cortex®-M3)**
- **Secure boot with RSA digital signature verification from eMMC and SPI NOR Flash**
- **On chip 32Kbit OTP**
- **True random number generator**
- **DRM engine supports**
 - AES, DES, 3DES, RSA, ECC
- **Disable / enable JTAG through authentication**
- **Memory and I/O space access control**
- **DRAM scrambling support**

Audio / Video Outputs

- **MIPI DSISM v1.2 output**
 - 1 x 4-lane
 - Supports up to 2160p30
- **One HDMI v2.1 output**
 - HDMI 2.1-compliant HDR schemes, including HDR10+
 - Up to 2160p60 YUV 4:4:4
 - Up to 1080p60 with 12b deep color
 - HDCP 2.3
 - HBR output
 - CEC
 - ARC Rx and eARC Rx
 - Variable Refresh Rate (VRR)
 - Auto Lip Sync Correction
 - Supports Quick Media Switching (QMS), Quick Frame Transport (QFT), and Auto Low-Latency Mode (ALLM)

- 8-channel I²S output
- 2-channel I²S/PCM output or 8-channel TDM output
- S/PDIF output

Audio / Video Inputs

- MIPI CSI2SM v1.2 input
 - 1 x 2-lane, 1 x 4-lane
 - Supports up to 2160p60 (one camera) or 2 x 2160p30 (two cameras)
 - 8MP + 4MP dual-sensor support
 - Integrated ISP
 - Up to two cameras support
 - Input pixel format: RAW (RGGB), 10/12-bit per pixel
 - Output pixel format: YUV420/422/444, 8/10-bit; RGB444, 8/10-bit; RAW, 10/12-bit
- One HDMI v2.1 input
 - HDR10 and HLG
 - Up to 2160p60 YUV 4:4:4
 - Up to 1080p60 with 12b deep color
 - HDCP 2.3
 - HBR audio input
 - CEC
 - Dynamic HDR Metadata feature / HDR10+
 - Variable Refresh Rate (VRR)
 - Auto Lip Sync Correction
 - Supports Quick Media Switching (QMS), Quick Frame Transport (QFT), Auto Low-Latency Mode (ALLM)
- 8-channel I²S
- 2-channel I²S/PCM input or 8-channel TDM input
- 4 x 2-channel PDM (microphone) input
- S/PDIF input

Standby Mode System Manager

- 25MHz Arm[®] Cortex[®]-M3 (ARMv7-M compatible)
- 128KB TCM for instruction/data, 4KB secure RAM
- Separate power island with front panel controlling I/O, ADC, SPI, UART, Temperature sensor and wake-up event logic
- Multiple GPIOs in standby mode
- Always-on domain to support system wake-up events:
 - Wake-on-Voice

- Wake-on-LAN
- Wake-on-CEC
- IR remote
- Front-panel key presses through ADC or GPIO
- Wake-on-Wi-Fi through GPIO
- Wake-on-Bluetooth[®] through GPIO
- ZigBee through GPIO
- Timer

Peripherals

- One dual-lane PCI Express[®] 2.0 root complex
- One Gigabit Ethernet MAC
 - RGMII interface for connection to an external Gb Ethernet PHY or G.hn
- One USB 3.0 host interface
- One USB 2.0 On-The-Go (OTG) interface
- One SDIO 3.01 host interface up to 200 MHz
- Four TWSI 2-wire bus (I2C compatible)
- Two high-speed UART interfaces
- Two low-speed UART interfaces (in always-on power domain)
- Two SPI interfaces (one with DMA)
- 32-bit pin-shared standby domain GPIOs
- 96-bit pin-shared standard mode GPIOs
- Four PWM
- Single-channel 100kHz front panel ADC
- IR receiver input
- Two on-chip temperature sensors

Power, Package and Layout

- Package: 17mm x 17mm
 - FCBGA, 0.4mm ball pitch
 - Ball pattern supports standard PCB fab rules (no HDI rules required)

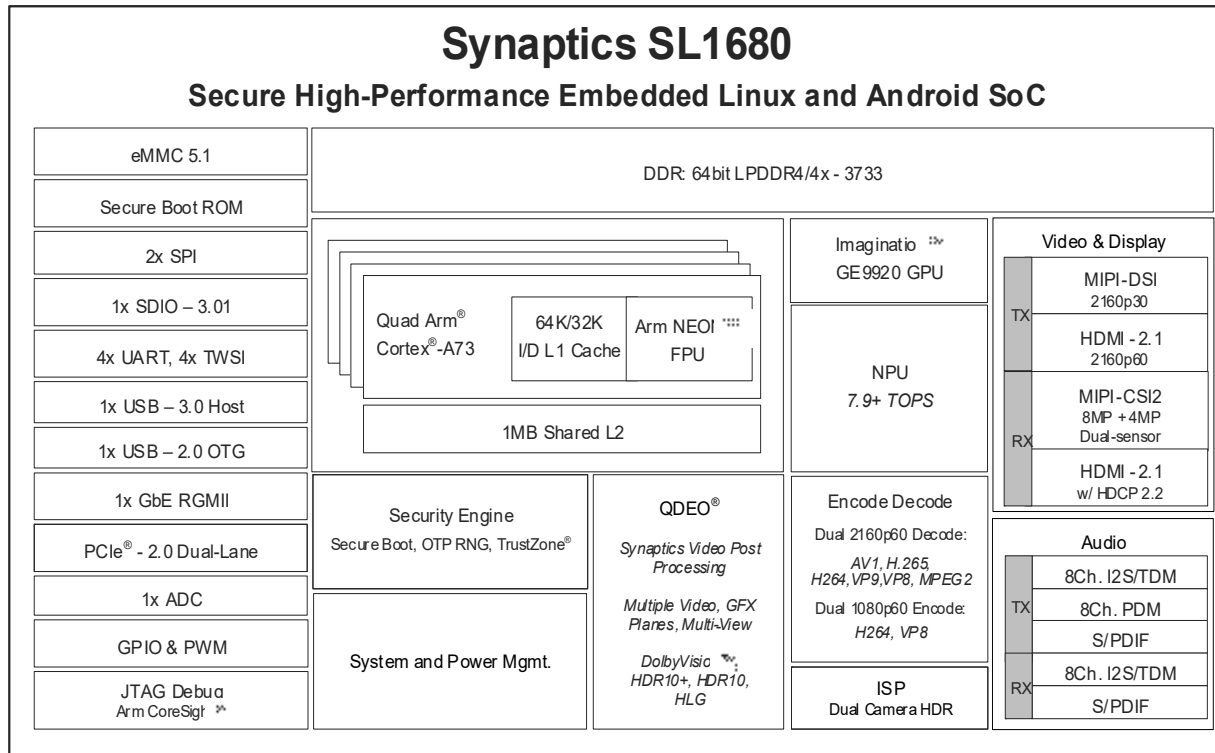


Figure 1. SL1680 High-level block diagram

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1. Signal Description

Table 1. Pin Type Definitions

| Pin Type | Definitions |
|----------|---|
| I | Input only |
| O | Output only |
| I/O | Input and output |
| Analog | Analog Pin |
| CMOS | Complementary metal oxide semiconductor |
| SSTL | Stub Series Terminated Logic |
| PWR | Power Supply |
| GND | Ground Pin |
| Iu | Input with internal pull-up |
| Id | Input with internal pull-down |
| I/Ood | Input/Output pin, Open-Drain type |
| I/Ouod | Input/Output pin with internal pull-up, Open-Drain type |
| I/Odod | Input/Output pin with internal pull-down, Open-Drain type |
| Ouod | Output pin with internal pull-up, Open-Drain type |
| Ou | Output pin with internal pull-up |
| Od | Output pin with internal pull-down |

Note: A lowercase n at the end of a signal name indicates an active-low signal.

Table 2. Interface Prefixes

| Pin Type | Definitions |
|-----------------------------------|--------------------|
| TWSI | TW_ |
| System Manager | SM_ |
| LPDDR4 memory channel 0, 1, 2, 3 | M0_, M1_, M2_, M3_ |
| Serial transport stream interface | STS0_, STS1_ |

1.1. SL1680 Pinout

Due to the large number of pins, the package is depicted graphically over the following 6 pages.

Table 3. SL1680 Pinouts Top View (1 of 6)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|----|---------------|---------------|---------------|-----------|-------------------|----------|-------------------|-----------|----------------|----|
| A | VSS | VSS | M1_DQ[8] | | | | | | | A |
| B | VSS | VSS | M1_DQ[10] | M1_DM[1] | | | | | | B |
| C | M2_DQ[3] | M2_DQ[0] | | M1_DQ[11] | | M1_DQ[9] | | M1_DQ[13] | | C |
| D | | M2_DM[0] | M2_DQ[1] | | | | | | | D |
| E | | | | | | | VSS | | | E |
| F | | | M2_DQ[2] | | | | | | | F |
| G | | | | | VSS | | | | | G |
| H | | | M2_DQ[4] | | | | | | | H |
| J | | | | | | | | | | J |
| K | M2_DQ[6] | M2_DQ[5] | VSS | | | | | | | K |
| L | | M2_DQ[7] | M2_DQ[10] | | VSS | | M2_DQ[8] | | VSS | L |
| M | | | M2_DQ[14] | | | | | | | M |
| N | | | | | | | | | | N |
| P | | | M2_DM[1] | | | | | | | P |
| R | | | | | M2_DQ[9] | | M2_DQ[11] | | M2_DQSN[0] | R |
| T | M2_DQ[13] | M2_DQ[15] | VSS | | | | | | | T |
| V | | M2_CSN | M2_CKE | | | | | | | V |
| W | | | M2_A[3] | | VSS | | M2_DQ[12] | | M2_DQSN[1] | W |
| Y | | | M2_A[5] | | | | | | | Y |
| AB | M2_A[4] | M2_A[1] | VSS | | | | | | | AB |
| AC | | | | | VSS | | M2_A[2] | | M2_CKN | AC |
| AD | | M3_CKE | M3_CSN | | | | | | | AD |
| AF | | | M3_A[0] | | | | | | | AF |
| AG | | | M3_A[3] | | M3_A[2] | | M3_A[1] | | VSS | AG |
| AH | M3_A[5] | M3_DQ[3] | VSS | | | | | | | AH |
| AK | | M3_DQ[1] | M3_DQ[0] | | | | | | | AK |
| AL | | | | | VSS | | M3_A[4] | | M3_CKN | AL |
| AM | | | M3_DQ[2] | | | | | | | AM |
| AP | | | M3_DM[0] | | | | | | | AP |
| AR | M3_DQ[7] | M3_DQ[5] | VSS | | VSS | | M3_DQ[4] | | M3_DQSN[0] | AR |
| AT | | M3_DQ[6] | M3_DQ[11] | | | | | | | AT |
| AV | | | M3_DQ[10] | | | | | | | AV |
| AW | | | | | M3_DQ[9] | | M3_DQ[12] | | M3_DQSP[1] | AW |
| AY | | | M3_DQ[8] | | | | | | | AY |
| BB | M3_DM[1] | M3_DQ[14] | VSS | | | | | | | BB |
| BC | | M3_DQ[15] | M3_DQ[13] | | VSS | | MIPI_CSIO_ATB | | MIPI_CSIO_REXT | BC |
| BD | | | MIPI_CSIO_D2N | | | | | | | BD |
| BF | | | MIPI_CSIO_D2P | | | | | | | BF |
| BG | | | | | MIPI_CSIO_AVDD1P8 | | VSS | | MIPI_CSI1_REXT | BG |
| BH | MIPI_CSIO_D3N | MIPI_CSIO_D3P | VSS | | | | | | | BH |
| BJ | | | | | | | | | | BJ |
| BK | | MIPI_CSIO_D1P | MIPI_CSIO_D1N | | | | | | | BK |
| BL | | | MIPI_CSIO_D0N | | VSS | | MIPI_CSI1_AVDD1P8 | | USB2_REXT | BL |
| BM | | | MIPI_CSIO_D0P | | | | | | | BM |
| BN | | | | | | | | | | BN |
| BP | MIPI_CSIO_CKP | MIPI_CSIO_CKN | VSS | | | | | | | BP |
| BR | | | | | VSS | | USB2_AVDD3P3 | | | BR |
| BT | | MIPI_CSI1_D0P | MIPI_CSI1_D0N | | | | | | | BT |
| BU | | | | | | | USB2_VR_AVDD3P3 | | | BU |
| BV | | | MIPI_CSI1_D1N | | | | | | | BV |
| BW | | | MIPI_CSI1_D1P | USB2_DP | | USB3_RXP | | USB3_RXN | | BW |
| BY | VSS | VSS | MIPI_CSI1_CKN | USB2_DN | | | | | | BY |
| CA | VSS | VSS | MIPI_CSI1_CKP | | | | | | | CA |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |

Table 4. SL1680 Pinouts Top View (2 of 6)

| | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 18 | 19 | |
|----|-----------|----------------|-----------|----------------|-----------|------------|-----------------|-----------|-----------------|----|
| A | M1_DQ[14] | | | | | | M1_DQ[5] | | | A |
| B | M1_DQ[15] | M1_DQ[3] | | | | | M1_DQ[4] | M1_DQ[7] | | B |
| C | VSS | M1_DQ[0] | M1_DQ[2] | | M1_DQ[1] | | VSS | M1_DQ[6] | M1_A[2] | C |
| D | | | | | | | | | | D |
| E | | VSS | | | | M1_DM[0] | | | VSS | E |
| F | | | | | | | | | | F |
| G | | M1_DQ[12] | | | | VSS | | | M1_A[3] | G |
| H | | | | | | | | | | H |
| J | | VSS | | | | M1_DQSP[1] | | | M1_DQSN[0] | J |
| K | | | | | | | | | | K |
| L | | VSS | | | | M1_DQSN[1] | | | M1_DQSP[0] | L |
| M | | | | | | | | | | M |
| N | | | | VSS | | VDDQ | | | VDDQ | N |
| P | | | | | | | | | | P |
| R | | M2_DQSP[0] | | | | | | | | R |
| T | | | | | | | | | | T |
| V | | | | | | | VDDQ | | VSS | V |
| W | | M2_DQSP[1] | | VDDQ | | | | | | W |
| Y | | | | | | | VSS | | VDDQLP | Y |
| AB | | | | | | | | | | AB |
| AC | | M2_CKP | | M2_A[0] | | | | | | AC |
| AD | | | | | | | VSS | | MO_AVDD1P8 | AD |
| AF | | | | | | | | | VDDQLP | AF |
| AG | | M2_CAL | | VDDQ | | | VSS | | VDDQLP | AG |
| AH | | | | | | | | | | AH |
| AK | | | | | | | VSS | | VDDQ | AK |
| AL | | M3_CKP | | M2_RSTN | | | | | | AL |
| AM | | | | | | | VSS | | VDDQ | AM |
| AP | | | | | | | | | | AP |
| AR | | M3_DQSP[0] | | VSS | | | VDDQ | VDDQ | VDDQLP | AR |
| AT | | | | | | | | | VDDQLP | AT |
| AV | | | | | | | VSS | | VDD_CORE | AV |
| AW | | M3_DQSN[1] | | VSS | | | | | | AW |
| AY | | | | | | | | | | AY |
| BB | | | | | | | VDD_CORE | | VSS | BB |
| BC | | MIPI_CSIO_AVDD | | VSS | | | | | | BC |
| BD | | | | | | | KILOOTP_AVDD1P8 | | VDD_CORE | BD |
| BF | | | | | | | | VDD_CORE | | BF |
| BG | | VSS | | MIPI_CSI1_AVDD | | | | | | BG |
| BH | | | | | | | | | | BH |
| BJ | | | | | | VSS | | | VDD_CORE | BJ |
| BK | | | | | | | | | | BK |
| BL | | USB2_VBUS | | USB2_ID | | USB3_AVDD | | | VSS | BL |
| BM | | | | | | | | | | BM |
| BN | | USB2_DVDD | | | | VSS | | | VSS | BN |
| BP | | | | | | | | | | BP |
| BR | | USB3_AVDD3P3 | | | | USB3_DVDD | | | PCIE_TX_AVDD[1] | BR |
| BT | | | | | | | | | | BT |
| BU | | VSS | | | | PCIE_AVDD | | | VSS | BU |
| BV | | | | | | | | | | BV |
| BW | VSS | USB3_DN | PCIE_RX1P | | PCIE_RX1N | | VSS | PCIE_RX0N | PCIE_TX0N | BW |
| BY | USB3_TXN | USB3_DP | | | | | PCIE_TX1P | PCIE_RX0P | | BY |
| CA | USB3_TXP | | | | | | PCIE_TX1N | | | CA |
| | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 18 | 19 | |

Table 5. SL1680 Pinouts Top View (3 of 6)

| | 20 | 22 | 23 | 24 | 26 | 27 | 28 | 30 | 31 | 32 | |
|----|-----------|-----------|-----------------|--------------|--------------|------------------|--------------|--------------|------------------|--------------|----|
| A | | M1_A[4] | | | | | MO_CKE | | | | A |
| B | | M1_A[0] | | M1_CSN | | | MO_CSN | MO_DQ[10] | | | B |
| C | M1_A[5] | VSS | | M1_CKE | MO_A[3] | MO_A[2] | VSS | MO_DQ[11] | | MO_DM[1] | C |
| D | | | | | | | | | | | D |
| E | | | VSS | | | MO_A[5] | | | VSS | | E |
| F | | | | | | | | | | | F |
| G | | | M1_A[1] | | | MO_A[4] | | | MO_A[0] | | G |
| H | | | | | | | | | | | H |
| J | | | M1_CKN | | | MO_RSTN | | | MO_CKP | | J |
| K | | | | | | | | | | | K |
| L | | | M1_CKP | | | MO_CAL | | | MO_CKN | | L |
| M | | | | | | | | | | | M |
| N | | | MO_VREF | | | VDDQ | | | MO_A[1] | | N |
| P | | | | | | | | | | | P |
| R | | | | | | | | | | | R |
| T | | | | | | | | | | | T |
| V | | VSS | | | VSS | | VSS | | | VDD_CPU | V |
| W | | | | | | | | | | | W |
| Y | | VDDQ | | | VDDQLP | | VDDQ | VDDQ | | VSS | Y |
| AB | | | | | | | | | | | AB |
| AC | | | | | | | | | | | AC |
| AD | | VSS | | | VDDQLP | | VDDQLP | | | VDD_CPU | AD |
| AF | | | | | | | | | | | AF |
| AG | | VSS | | | VDD_CORE | | VSS | | | VDD_CORE | AG |
| AH | | | | | | | | | | | AH |
| AK | | VSS | | | VDD_CORE | | VSS | | | VDD_CORE | AK |
| AL | | | | | | | | | | | AL |
| AM | | VSS | | | VDD_CORE | | VSS | | | VDD_CORE | AM |
| AP | | | | | | | | | | | AP |
| AR | | VDD_CORE | | | VSS | VSS | VDD_CORE | | | VSS | AR |
| AT | | | | | | | | | | | AT |
| AV | | VSS | | | VDD_CORE | | VSS | | | VDD_CORE | AV |
| AW | | | | | | | | | | | AW |
| AY | | | | | | | | | | | AY |
| BB | | VDD_CORE | | | VSS | | VDD_CORE | | | VSS | BB |
| BC | | | | | | | | | | | BC |
| BD | | VSS | | | VDD_CORE | | VSS | | | VDD_CORE | BD |
| BF | | | | | | | | | | | BF |
| BG | | | | | | | | | | | BG |
| BH | | | | | | | | | | | BH |
| BJ | | | VSS | | | VDD_CORE | | | VSS | | BJ |
| BK | | | | | | | | | | | BK |
| BL | | | USB3_REXT | | | USB3_ID | | | PCIE_REXT | | BL |
| BM | | | | | | | | | | | BM |
| BN | | | USB3_VBUS | | | PCIE_PLL_AVSS | | | VSS | | BN |
| BP | | | | | | | | | | | BP |
| BR | | | PCIE_TX_AVDD[0] | | | PCIE_PLL_AVDD1P8 | | | PCIE_REFCLK_AVDD | | BR |
| BT | | | | | | | | | | | BT |
| BU | | | VSS | | | PCIE_AVDD1P8 | | | VSS | | BU |
| BV | | | | | | | | | | | BV |
| BW | PCIE_TXOP | VSS | | MIPI_DSI_D0P | MIPI_DSI_D1N | MIPI_DSI_D1P | VSS | MIPI_DSI_D3P | | MIPI_DSI_D2P | BW |
| BY | | PCIE_CLKN | | MIPI_DSI_D0N | | | MIPI_DSI_CKN | MIPI_DSI_D3N | | | BY |
| CA | | PCIE_CLKP | | | | | MIPI_DSI_CKP | | | | CA |
| | 20 | 22 | 23 | 24 | 26 | 27 | 28 | 30 | 31 | 32 | |

Table 6. SL1680 Pinouts Top View (4 of 6)

| | 34 | 35 | 36 | 38 | 39 | 40 | 42 | 43 | |
|----|--------------|---------------|-------------|-------------|------------------|-------------|-------------|----------------|----|
| A | | MO_DQ[14] | | | | | MO_DQ[5] | | A |
| B | | MO_DQ[12] | MO_DQ[15] | | | | MO_DM[0] | MO_DQ[7] | B |
| C | MO_DQ[8] | VSS | MO_DQ[13] | MO_DQ[3] | | MO_DQ[2] | VSS | MO_DQ[6] | C |
| D | | | | | | | | | D |
| E | | VSS | | | MO_DQ[0] | | | VSS | E |
| F | | | | | | | | | F |
| G | | MO_DQ[9] | | | MO_DQ[1] | | | SDIO_VDDIO1P8 | G |
| H | | | | | | | | | H |
| J | | MO_DQSP[1] | | | MO_DQSP[0] | | | MEMPLL_AVDD1P8 | J |
| K | | | | | | | | | K |
| L | | MO_DQSN[1] | | | MO_DQSN[0] | | | MEMPLL_AVSS | L |
| M | | | | | | | | | M |
| N | | VSS | | | MO_DQ[4] | | | SDIO_DATA[0] | N |
| P | | | | | | | | | P |
| R | | | | | | | | | R |
| T | | | | | | | | | T |
| V | | VSS | | VDD_CPU | | | VSS | | V |
| W | | | | | | | | | W |
| Y | VSS | VDD_CPU | | VSS | | | VDD_CPU | | Y |
| AB | | | | | | | | | AB |
| AC | | | | | | | | | AC |
| AD | | VSS | | VDD_CPU | | | VSS | | AD |
| AF | | | | | | | | | AF |
| AG | VSS | VDD_CPU | | VSS | | | VDD_CPU | | AG |
| AH | | | | | | | | | AH |
| AK | | VSS | | VDD_CPU | | | VSS | | AK |
| AL | | | | | | | | | AL |
| AM | | VSS | | VDD_CORE | | | VSS | | AM |
| AP | | | | | | | | | AP |
| AR | | VDD_CORE | | VSS | | VSS | VDD_CORE | | AR |
| AT | | | | | | | | | AT |
| AV | | VSS | | VDD_CORE | | | VSS | | AV |
| AW | | | | | | | | | AW |
| AY | | | | | | | | | AY |
| BB | | VDD_CORE | | VSS | | | VDD_CORE | | BB |
| BC | | | | | | | | | BC |
| BD | | VSS | | VDD_CORE | | | VSS | | BD |
| BF | | | | | | | | | BF |
| BG | | | | | | | | | BG |
| BH | | | | | | | | | BH |
| BJ | | VDD_CORE | | | VSS | | | HDMI_TX_HPD | BJ |
| BK | | | | | | | | | BK |
| BL | | MIPI_DSI_REXT | | | HDMI_RX_REXT | | | HDMI_TX_REXT | BL |
| BM | | | | | | | | | BM |
| BN | | MIPI_DSI_ATB | | | VSS | | | HDMI_RX_DVDD | BN |
| BP | | | | | | | | | BP |
| BR | | MIPI_DSI_AVDD | | | NC | | | NC | BR |
| BT | | | | | | | | | BT |
| BU | | VSS | | | MIPI_DSI_AVDD1P8 | | | VSS | BU |
| BV | | | | | | | | | BV |
| BW | MIPI_DSI_D2N | VSS | HDMI_RX_CKP | HDMI_RX_DON | | HDMI_RX_DOP | VSS | HDMI_RX_D2P | BW |
| BY | | NC | HDMI_RX_CKN | | | | HDMI_RX_D1P | HDMI_RX_D2N | BY |
| CA | | NC | | | | | HDMI_RX_D1N | | CA |
| | 34 | 35 | 36 | 38 | 39 | 40 | 42 | 43 | |

Table 7. SL1680 Pinouts Top View (5 of 6)

| | 44 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | |
|----|--------------|--------------|-------------------|---------------|------------------|--------------|----------------------|-------------|----|
| A | | | | SDIO_VDDIO3P3 | | | | | A |
| B | | | | SDIO_CLK | | SDIO_CMD | | | B |
| C | SDIO_DATA[1] | SDIO_DATA[2] | | VSS | | EMMC_DATA[6] | EMMC_RSTN | EMMC_CMD | C |
| D | | | | | | | | | D |
| E | | | VSS | | | | EMMC_VDDIO1P8 | | E |
| F | | | | | | | | | F |
| G | | | SDIO_DATA[3] | | | | VSS | | G |
| H | | | | | | | | | H |
| J | | | SDIO_CDN | | | | CPUPLL_AVDD1P8 | | J |
| K | | | | | | | | | K |
| L | | | SDIO_WP | | | | CPUPLL_AVSS | | L |
| M | | | | | | | | | M |
| N | | | VSS | | VSS | | | | N |
| P | | | | | | | | | P |
| R | | | CPUTSEN_AVDD1P8 | | | | STS0_SOP | | R |
| T | CPUTSEN_AVSS | | | | | | | | T |
| V | VSS | | | | | | | | V |
| W | | | STS0_CLK | | STS0_SD | | VSS | | W |
| Y | VSS | | | | | | | | Y |
| AB | | | | | | | | | AB |
| AC | | | TWO_SCL | | TWO_SDA | | RGMII_TXCTL | | AC |
| AD | VDD_CPU | | | | | | | | AD |
| AF | | | | | | | | | AF |
| AG | VSS | | RGMII_TXD[1] | | RGMII_RXC | | RGMII_RXD[3] | | AG |
| AH | | | | | | | | | AH |
| AK | VDD_CPU | | | | | | | | AK |
| AL | | | SM_VDDIO1P8 | | SM_POR_EN | | SM_TRSTN | | AL |
| AM | VDD_CORE | | | | | | | | AM |
| AP | | | | | | | | | AP |
| AR | VSS | | SM_VDD_CORE | | VSS | | SM_TW3_SCL | | AR |
| AT | | | | | | | | | AT |
| AV | VDD_CORE | | | | | | | | AV |
| AW | | | SM_RCLKO | | SM_RCLKI | | SM_URTO_RXD | | AW |
| AY | | | | | | | | | AY |
| BB | SM_TSEN_AVSS | | | | | | | | BB |
| BC | | | SM_TSEN_AVDD1P8 | | SM_ADC_AVSS | | SM_ADC_AVDD1P8 | | BC |
| BD | VDD_CORE | | | | | | | | BD |
| BF | | | | | | | | | BF |
| BG | | | SYSPLL_AVSS | | SYSPLL_AVDD1P8 | | VSS | | BG |
| BH | | | | | | | | | BH |
| BJ | | | HDMI_TX_HEAC_AVDD | | | | | | BJ |
| BK | | | | | | | | | BK |
| BL | | | VSS | | HDMI_TX_EDDC_SCL | | HDMI_TX_EDDC_SDA | | BL |
| BM | | | | | | | | | BM |
| BN | | | HDMI_RX_AVDD1P8 | | | | HDMI_TX_HEAC_AVDD1P8 | | BN |
| BP | | | | | | | | | BP |
| BR | | | HDMI_RX_AVDD3P3 | | | | VSS | | BR |
| BT | | | | | | | | | BT |
| BU | | | VSS | | | | HDMI_RX_AVDD | | BU |
| BV | | | | | | | | | BV |
| BW | HDMI_TX_CKN | HDMI_TX_CKP | | VSS | | | HDMI_TX_AVDD | | BW |
| BY | | | | HDMI_TX_D0P | | HDMI_TX_D1N | HDMI_TX_D1P | HDMI_TX_D2P | BY |
| CA | | | | HDMI_TX_D0N | | | | HDMI_TX_D2N | CA |
| | 44 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | |

Table 8. SL1680 Pinouts Top View (6 of 6)

| | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | |
|----|---------------|---------------|---------------|---------------|-----------------|-------------------|--------------|----------------|------------------|----|
| A | | EMMC_CLK | | | | | | VSS | VSS | A |
| B | | EMMC_DATA[5] | | EMMC_STRB | | | | VSS | VSS | B |
| C | | VSS | | EMMC_DATA[2] | | EMMC_DATA[7] | EMMC_DATA[1] | EMMC_DATA[4] | EMMC_DATA[3] | C |
| D | | | | | | | EMMC_DATA[0] | | | D |
| E | | | VSS | | | | | | | E |
| F | | | | | | | SPI1_SS1N | | | F |
| G | | | | | VSS | | | | | G |
| H | | | | | | | SPI1_SS0N | SPI1_SS3N | | H |
| J | | | | | | | | | | J |
| K | | | | | | | VSS | SPI1_SS2N | SPI1_SDO | K |
| L | VDDIO1P8 | | VDDIO1P8 | | VSS | | SPI1_SCLK | | | L |
| M | | | | | | | SPI1_SDI | | | M |
| N | | | | | | | | | | N |
| P | | | | | | | STS1_SD | STS1_VALD | | P |
| R | STS0_VALD | | STS1_SOP | | STS1_CLK | | | | | R |
| T | | | | | | | VSS | RGMII_MDC | RGMII_TXC | T |
| V | | | | | | | RGMII_TXD[0] | | | V |
| W | USB2_DRV_VBUS | | RGMII_MDIO | | VSS | | RGMII_TXD[2] | | | W |
| Y | | | | | | | RGMII_TXD[3] | RGMII_RXD[2] | | Y |
| AB | | | | | | | VSS | SM_URT1_RXD | RGMII_RXD[1] | AB |
| AC | RGMII_RXD[0] | | RGMII_RXCTL | | VSS | | | | | AC |
| AD | | | | | | | SM_TW2_SDA | | | AD |
| AF | | | | | | | SM_TW2_SCL | | | AF |
| AG | VSS | | VDD_CPU_FB | | VDD_CORE_FB | | SM_URT1_TXD | SM_HDMI_TX_HPD | | AG |
| AH | | | | | | | VSS | SM_HDMI_CEC | SM_JTAG_SEL | AH |
| AK | | | | | | | SM_TEST_EN | | | AK |
| AL | VSS | | SM_RSTIN | | VSS | | | | | AL |
| AM | | | | | | | SM_TCK | | | AM |
| AP | | | | | | | SM_TMS | SM_TDI | | AP |
| AR | SM_TW3_SDA | | SM_SPI2_SS1N | | VSS | | VSS | SM_TDO | SM_SPI2_SS0N | AR |
| AT | | | | | | | SM_SPI2_SS2N | | | AT |
| AV | | | | | | | SM_SPI2_SCLK | | | AV |
| AW | VSS | | SM_URT0_TXD | | SM_SPI2_SDI | | | | | AW |
| AY | | | | | | | SM_SPI2_SS3N | SM_SPI2_SDO | | AY |
| BB | | | | | | | VSS | SM_HDMI_RX_HPD | SM_HDMI_RX_PWR5V | BB |
| BC | SM_ADCI[1] | | SM_ADCI[0] | | SM_OSC_VDDIO1P8 | | VSS | | | BC |
| BD | | | | | | | I2S1_DO[0] | | | BD |
| BF | | | | | | | I2S1_DO[3] | I2S1_DO[1] | | BF |
| BG | I2S1_MCLK | | I2S1_LRCK | | VSS | | | | | BG |
| BH | | | | | | | VSS | I2S1_BCLK | I2S1_DO[2] | BH |
| BJ | | | | | | | | | | BJ |
| BK | | | | | | | SPDIFO | | | BK |
| BL | VSS | | VDDIO1P8 | | VDDIO1P8 | | SPDIFI | | | BL |
| BM | | | | | | | I2S2_DI[1] | I2S2_LRCK | | BM |
| BN | | | AVPLL_AVSS | | | | | | | BN |
| BP | | | | | | | VSS | I2S2_BCLK | I2S2_MCLK | BP |
| BR | | | AVPLL_AVDD1P8 | | VSS | | | | | BR |
| BT | | | | | | | I2S2_DI[0] | I2S2_DI[3] | I2S2_DI[2] | BT |
| BU | | | VSS | | HDMI_TX_AVDD1P8 | | | | | BU |
| BV | | | | | | | I2S3_LRCK | | | BV |
| BW | | | | | | | | | | BW |
| BY | | HDMI_TX_HEACN | | HDMI_TX_HEACP | | HDMI_TX_HEAC_REXT | I2S3_DO | VSS | VSS | BY |
| CA | | | | | | I2S3_BCLK | I2S3_DI | VSS | VSS | CA |
| | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | |

1.2. Pin Descriptions

Table 9. USB2.0 Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------------|-------------|--|
| BW4 | USB2_Dp | I/O, Analog | USB 2.0 port data positive. |
| BY4 | USB2_Dn | I/O, Analog | USB 2.0 port data negative. |
| W53 | USB2_DRV_VBUS | O, CMOS | USB OTG requires this signal. It enables 5V to be driven onto VBUS. 0 = Do not drive VBUS. 1 = Drive 5V on VBUS. DRV_VBUS must be connected to an external PMIC chip to provide power for USB VBUS. There is no on-chip power switch for VBUS inside the PHY. |
| BL13 | USB2_ID | I, Analog | USB 2.0 Port OTG ID pin. This pin should be left floating or connected to GND. |
| BL9 | USB2_REXT | I, Analog | USB 2.0 Calibration pad. This pin should be connected to VSS via a 200 ohm resistor. |
| BL11 | USB2_VBUS | I, Analog | USB 2.0 VBUS. This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30Kohm resistor so it could see a lower voltage. |

Table 10. USB3.0 Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|-------------|---|
| BY11 | USB3_Dp | I/O, Analog | USB 3.0 port data positive. |
| BW11 | USB3_Dn | I/O, Analog | USB 3.0 port data negative. |
| BL27 | USB3_ID | I, Analog | USB 3.0 port 0 ID pin. This pin should be left floating or connected to GND. |
| BL23 | USB3_REXT | I, Analog | USB 3.0 Calibration pad. This pin should be connected to VSS via a 200 ohm resistor. |
| BW6 | USB3_RXp | I, Analog | USB 3.0 port receive positive. |
| BW8 | USB3_RXn | I, Analog | USB 3.0 port receive negative. |
| CA10 | USB3_TXp | O, Analog | USB 3.0 port transmit positive. |
| BY10 | USB3_TXn | O, Analog | USB 3.0 port transmit negative. |
| BN23 | USB3_VBUS | I, Analog | USB 3.0 port 0 VBUS. This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30Kohm resistor so it could see a lower voltage. |

Table 11. HDMI Receiver PHY Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-------------------------|-----------|--|
| BL39 | HDMI_RX_REXT | I, Analog | HDMI RX Calibration pad. This pin should be connected to VSS via a 200 ohm resistor. |
| BY36 | HDMI_RX_CK _n | I, Analog | TMDS clock negative. |
| BW36 | HDMI_RX_CK _p | I, Analog | TMDS clock positive. |
| BW38 | HDMI_RX_D0 _n | I, Analog | TMDS data 0 negative. |
| BW40 | HDMI_RX_D0 _p | I, Analog | TMDS data 0 positive. |
| CA42 | HDMI_RX_D1 _n | I, Analog | TMDS data 1 negative. |
| BY42 | HDMI_RX_D1 _p | I, Analog | TMDS data 1 positive. |
| BY43 | HDMI_RX_D2 _n | I, Analog | TMDS data 2 negative. |
| BW43 | HDMI_RX_D2 _p | I, Analog | TMDS data 2 positive. |

Table 12. HDMI Transmitter PHY Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------------------------|-----------|---|
| BY54 | HDMI_TX_HEAC _n | I, Analog | HDMI Ethernet and audio return channel negative. |
| BY56 | HDMI_TX_HEAC _p | I, Analog | HDMI Ethernet and audio return channel positive. |
| BY58 | HDMI_TX_HEAC_REXT | I, Analog | HDMI TX eARC calibration pad. Connect to VSS via a 2.4 kohm resistor. |
| BL43 | HDMI_TX_REXT | I, Analog | HDMI TX Calibration pad. This pin should be connected to VSS via a 1.62 kohm \pm 1% resistor. |
| BJ43 | HDMI_TX_HPD | I, CMOS | HDMI TX hot plug detect. This pin is 5V tolerant. 1=Detect. |
| BW44 | HDMI_TX_CK _n | O, Analog | TMDS clock negative. |
| BW46 | HDMI_TX_CK _p | O, Analog | TMDS clock positive. |
| CA48 | HDMI_TX_D0 _n | O, Analog | TMDS data 0 negative. |
| BY48 | HDMI_TX_D0 _p | O, Analog | TMDS data 0 positive. |
| BY50 | HDMI_TX_D1 _n | O, Analog | TMDS data 1 negative. |
| BY51 | HDMI_TX_D1 _p | O, Analog | TMDS data 1 positive. |
| CA52 | HDMI_TX_D2 _n | O, Analog | TMDS data 2 negative. |
| BY52 | HDMI_TX_D2 _p | O, Analog | TMDS data 2 positive. |

Table 13. HDMI TX Enhanced DDC Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------------|-----------|---|
| BL49 | HDMI_TX_EDDC_SCL | I/O, CMOS | HDMI TX DDC serial clock line. This pin is 1.8V-only. |
| BL51 | HDMI_TX_EDDC_SDA | I/O, CMOS | HDMI TX DDC serial data line. This pin is 1.8V-only. |

Table 14. Serial Transport 0 Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|----------|--------------------------------------|
| W47 | STS0_CLK | I, CMOS | Serial TS capture serial data clock. |
| W49 | STS0_SD | I, CMOS | Serial TS capture serial data. |
| R51 | STS0_SOP | I, CMOS | Serial TS capture start of packet. |
| R53 | STS0_VALD | I, CMOS | Serial TS capture valid flag. |

Table 15. Serial Transport 1 Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|----------|--------------------------------------|
| R57 | STS1_CLK | I, CMOS | Serial TS capture serial data clock. |
| P59 | STS1_SD | I, CMOS | Serial TS capture serial data. |
| R55 | STS1_SOP | I, CMOS | Serial TS capture start of packet. |
| P60 | STS1_VALD | I, CMOS | Serial TS capture valid flag. |

Table 16. Audio I²S Interface and S/PDIF Output

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------|-----------|------------------------|
| BH60 | I2S1_BCLK | I/O, CMOS | Audio bit clock. |
| BD59 | I2S1_DO[0] | O, CMOS | Data output. |
| BF60 | I2S1_DO[1] | O, CMOS | Data output. |
| BH61 | I2S1_DO[2] | O, CMOS | Data output. |
| BF59 | I2S1_DO[3] | O, CMOS | Data output. |
| BG55 | I2S1_LRCK | I/O, CMOS | Audio WS or LR select. |
| BG53 | I2S1_MCLK | I/O, CMOS | MCLK input/output. |

Table 17. Audio I²S Interface 2

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------|-----------|------------------------|
| BP60 | I2S2_BCLK | I/O, CMOS | Audio bit clock. |
| BT59 | I2S2_DI[0] | I, CMOS | Data input. |
| BM59 | I2S2_DI[1] | I, CMOS | Data input. |
| BT61 | I2S2_DI[2] | I, CMOS | Data input. |
| BT60 | I2S2_DI[3] | I, CMOS | Data input. |
| BM60 | I2S2_LRCK | I/O, CMOS | Audio WS or LR select. |
| BP61 | I2S2_MCLK | Od, CMOS | MCLK output. |
| BL59 | SPDIFI | I, CMOS | S/PDIF input. |
| BK59 | SPDIFO | Ou, CMOS | S/PDIF output. |

Table 18. Audio I2S Interface 3

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|-----------|------------------------|
| CA58 | I2S3_BCLK | I/O, CMOS | Audio bit clock. |
| CA59 | I2S3_DI | I, CMOS | Data input. |
| BY59 | I2S3_DO | O, CMOS | Data output. |
| BV59 | I2S3_LRCK | I/O, CMOS | Audio WS or LR select. |

Table 19. LPDDR4 Interface Reset

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------|--------------|------------------------------|
| J27 | M0_RSTN | O, HS_LVCMOS | M0 RESETn for LPDDR4 SDRAMs. |
| AL13 | M2_RSTN | O, HS_LVCMOS | M2 RESETn for LPDDR4 SDRAMs. |

Table 20. LPDDR4 Interface M0 16-bit

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------------|----------------|-----------------------|
| J31 | MO_CKp | O, HS_LVCMOS | M0 clock positive. |
| L31 | MO_CKn | O, HS_LVCMOS | M0 clock negative. |
| A28 | MO_CKE | O, HS_LVCMOS | M0 clock enable. |
| B28 | MO_CS _n | O, HS_LVCMOS | M0 chip select. |
| G31 | MO_A[0] | O, HS_LVCMOS | M0 ADDR[0]. |
| N31 | MO_A[1] | O, HS_LVCMOS | M0 ADDR[1]. |
| C27 | MO_A[2] | O, HS_LVCMOS | M0 ADDR[2]. |
| C26 | MO_A[3] | O, HS_LVCMOS | M0 ADDR[3]. |
| G27 | MO_A[4] | O, HS_LVCMOS | M0 ADDR[4]. |
| E27 | MO_A[5] | O, HS_LVCMOS | M0 ADDR[5]. |
| B42 | MO_DM[0] | O, HS_LVCMOS | M0 Data mask BYTE[0]. |
| C32 | MO_DM[1] | O, HS_LVCMOS | M0 Data mask BYTE[1]. |
| E39 | MO_DQ[0] | I/O, HS_LVCMOS | M0 DQ[0]. |
| G39 | MO_DQ[1] | I/O, HS_LVCMOS | M0 DQ[1]. |
| C40 | MO_DQ[2] | I/O, HS_LVCMOS | M0 DQ[2]. |
| C38 | MO_DQ[3] | I/O, HS_LVCMOS | M0 DQ[3]. |
| N39 | MO_DQ[4] | I/O, HS_LVCMOS | M0 DQ[4]. |
| A42 | MO_DQ[5] | I/O, HS_LVCMOS | M0 DQ[5]. |
| C43 | MO_DQ[6] | I/O, HS_LVCMOS | M0 DQ[6]. |
| B43 | MO_DQ[7] | I/O, HS_LVCMOS | M0 DQ[7]. |
| C34 | MO_DQ[8] | I/O, HS_LVCMOS | M0 DQ[8]. |
| G35 | MO_DQ[9] | I/O, HS_LVCMOS | M0 DQ[9]. |
| B30 | MO_DQ[10] | I/O, HS_LVCMOS | M0 DQ[10]. |
| C30 | MO_DQ[11] | I/O, HS_LVCMOS | M0 DQ[11]. |
| B35 | MO_DQ[12] | I/O, HS_LVCMOS | M0 DQ[12]. |
| C36 | MO_DQ[13] | I/O, HS_LVCMOS | M0 DQ[13]. |
| A35 | MO_DQ[14] | I/O, HS_LVCMOS | M0 DQ[14]. |
| B36 | MO_DQ[15] | I/O, HS_LVCMOS | M0 DQ[15]. |
| J39 | MO_DQSp[0] | I/O, HS_LVCMOS | M0 DQSp[0] BYTE0. |
| J35 | MO_DQSp[1] | I/O, HS_LVCMOS | M0 DQSp[1] BYTE1. |
| L39 | MO_DQSn[0] | I/O, HS_LVCMOS | M0 DQSn[0] BYTE0. |
| L35 | MO_DQSn[1] | I/O, HS_LVCMOS | M0 DQSn[1] BYTE1. |

Table 21. LPDDR4 Interface M1 16-bit

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------------|----------------|-----------------------|
| L23 | M1_CKp | O, HS_LVCMOS | M1 clock positive. |
| J23 | M1_CKn | O, HS_LVCMOS | M1 clock negative. |
| C24 | M1_CKE | O, HS_LVCMOS | M1 clock enable. |
| B24 | M1_CS _n | O, HS_LVCMOS | M1 chip select. |
| B22 | M1_A[0] | O, HS_LVCMOS | M1 ADDR[0]. |
| G23 | M1_A[1] | O, HS_LVCMOS | M1 ADDR[1]. |
| C19 | M1_A[2] | O, HS_LVCMOS | M1 ADDR[2]. |
| G19 | M1_A[3] | O, HS_LVCMOS | M1 ADDR[3]. |
| A22 | M1_A[4] | O, HS_LVCMOS | M1 ADDR[4]. |
| C20 | M1_A[5] | O, HS_LVCMOS | M1 ADDR[5]. |
| E15 | M1_DM[0] | O, HS_LVCMOS | M1 data mask BYTE[0]. |
| B4 | M1_DM[1] | O, HS_LVCMOS | M1 data mask BYTE[1]. |
| C11 | M1_DQ[0] | I/O, HS_LVCMOS | M1 DQ[0]. |
| C14 | M1_DQ[1] | I/O, HS_LVCMOS | M1 DQ[1]. |
| C12 | M1_DQ[2] | I/O, HS_LVCMOS | M1 DQ[2]. |
| B11 | M1_DQ[3] | I/O, HS_LVCMOS | M1 DQ[3]. |
| B16 | M1_DQ[4] | I/O, HS_LVCMOS | M1 DQ[4]. |
| A16 | M1_DQ[5] | I/O, HS_LVCMOS | M1 DQ[5]. |
| C18 | M1_DQ[6] | I/O, HS_LVCMOS | M1 DQ[6]. |
| B18 | M1_DQ[7] | I/O, HS_LVCMOS | M1 DQ[7]. |
| A3 | M1_DQ[8] | I/O, HS_LVCMOS | M1 DQ[8]. |
| C6 | M1_DQ[9] | I/O, HS_LVCMOS | M1 DQ[9]. |
| B3 | M1_DQ[10] | I/O, HS_LVCMOS | M1 DQ[10]. |
| C4 | M1_DQ[11] | I/O, HS_LVCMOS | M1 DQ[11]. |
| G11 | M1_DQ[12] | I/O, HS_LVCMOS | M1 DQ[12]. |
| C8 | M1_DQ[13] | I/O, HS_LVCMOS | M1 DQ[13]. |
| A10 | M1_DQ[14] | I/O, HS_LVCMOS | M1 DQ[14]. |
| B10 | M1_DQ[15] | I/O, HS_LVCMOS | M1 DQ[15]. |
| L19 | M1_DQSp[0] | I/O, HS_LVCMOS | M1 DQSp[0] BYTE0. |
| J15 | M1_DQSp[1] | I/O, HS_LVCMOS | M1 DQSp[1] BYTE1. |
| J19 | M1_DQSn[0] | I/O, HS_LVCMOS | M1 DQSn[0] BYTE0. |
| L15 | M1_DQSn[1] | I/O, HS_LVCMOS | M1 DQSn[1] BYTE1. |

Table 22. LPDDR4 Interface M2 16-bit

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------------|----------------|-----------------------|
| AC11 | M2_CKp | O, HS_LVCMOS | M2 clock positive. |
| AC9 | M2_CKn | O, HS_LVCMOS | M2 clock negative. |
| V3 | M2_CKE | O, HS_LVCMOS | M2 clock enable. |
| V2 | M2_CS _n | O, HS_LVCMOS | M2 chip select. |
| AC13 | M2_A[0] | O, HS_LVCMOS | M2 ADDR[0]. |
| AB2 | M2_A[1] | O, HS_LVCMOS | M2 ADDR[1]. |
| AC7 | M2_A[2] | O, HS_LVCMOS | M2 ADDR[2]. |
| W3 | M2_A[3] | O, HS_LVCMOS | M2 ADDR[3]. |
| AB1 | M2_A[4] | O, HS_LVCMOS | M2 ADDR[4]. |
| Y3 | M2_A[5] | O, HS_LVCMOS | M2 ADDR[5]. |
| D2 | M2_DM[0] | O, HS_LVCMOS | M2 data mask BYTE[0]. |
| P3 | M2_DM[1] | O, HS_LVCMOS | M2 data mask BYTE[1]. |
| C2 | M2_DQ[0] | I/O, HS_LVCMOS | M2 DQ[0]. |
| D3 | M2_DQ[1] | I/O, HS_LVCMOS | M2 DQ[1]. |
| F3 | M2_DQ[2] | I/O, HS_LVCMOS | M2 DQ[2]. |
| C1 | M2_DQ[3] | I/O, HS_LVCMOS | M2 DQ[3]. |
| H3 | M2_DQ[4] | I/O, HS_LVCMOS | M2 DQ[4]. |
| K2 | M2_DQ[5] | I/O, HS_LVCMOS | M2 DQ[5]. |
| K1 | M2_DQ[6] | I/O, HS_LVCMOS | M2 DQ[6]. |
| L2 | M2_DQ[7] | I/O, HS_LVCMOS | M2 DQ[7]. |
| L7 | M2_DQ[8] | I/O, HS_LVCMOS | M2 DQ[8]. |
| R5 | M2_DQ[9] | I/O, HS_LVCMOS | M2 DQ[9]. |
| L3 | M2_DQ[10] | I/O, HS_LVCMOS | M2 DQ[10]. |
| R7 | M2_DQ[11] | I/O, HS_LVCMOS | M2 DQ[11]. |
| W7 | M2_DQ[12] | I/O, HS_LVCMOS | M2 DQ[12]. |
| T1 | M2_DQ[13] | I/O, HS_LVCMOS | M2 DQ[13]. |
| M3 | M2_DQ[14] | I/O, HS_LVCMOS | M2 DQ[14]. |
| T2 | M2_DQ[15] | I/O, HS_LVCMOS | M2 DQ[15]. |
| R11 | M2_DQSp[0] | I/O, HS_LVCMOS | M2 DQSp[0] BYTE0. |
| W11 | M2_DQSp[1] | I/O, HS_LVCMOS | M2 DQSp[1] BYTE1. |
| R9 | M2_DQSn[0] | I/O, HS_LVCMOS | M2 DQSn[0] BYTE0. |
| W9 | M2_DQSn[1] | I/O, HS_LVCMOS | M2 DQSn[1] BYTE1. |

Table 23. LPDDR4 Interface M3 16-bit

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------------|----------------|-----------------------|
| AL11 | M3_CKp | O, HS_LVCMOS | M3 clock positive. |
| AL9 | M3_CKn | O, HS_LVCMOS | M3 clock negative. |
| AD2 | M3_CKE | O, HS_LVCMOS | M3 clock enable. |
| AD3 | M3_CS _n | O, HS_LVCMOS | M3 chip select. |
| AF3 | M3_A[0] | O, HS_LVCMOS | M3 ADDR[0]. |
| AG7 | M3_A[1] | O, HS_LVCMOS | M3 ADDR[1]. |
| AG5 | M3_A[2] | O, HS_LVCMOS | M3 ADDR[2]. |
| AG3 | M3_A[3] | O, HS_LVCMOS | M3 ADDR[3]. |
| AL7 | M3_A[4] | O, HS_LVCMOS | M3 ADDR[4]. |
| AH1 | M3_A[5] | O, HS_LVCMOS | M3 ADDR[5]. |
| AP3 | M3_DM[0] | O, HS_LVCMOS | M3 data mask BYTE[0]. |
| BB1 | M3_DM[1] | O, HS_LVCMOS | M3 data mask BYTE[1]. |
| AK3 | M3_DQ[0] | I/O, HS_LVCMOS | M3 DQ[0]. |
| AK2 | M3_DQ[1] | I/O, HS_LVCMOS | M3 DQ[1]. |
| AM3 | M3_DQ[2] | I/O, HS_LVCMOS | M3 DQ[2]. |
| AH2 | M3_DQ[3] | I/O, HS_LVCMOS | M3 DQ[3]. |
| AR7 | M3_DQ[4] | I/O, HS_LVCMOS | M3 DQ[4]. |
| AR2 | M3_DQ[5] | I/O, HS_LVCMOS | M3 DQ[5]. |
| AT2 | M3_DQ[6] | I/O, HS_LVCMOS | M3 DQ[6]. |
| AR1 | M3_DQ[7] | I/O, HS_LVCMOS | M3 DQ[7]. |
| AY3 | M3_DQ[8] | I/O, HS_LVCMOS | M3 DQ[8]. |
| AW5 | M3_DQ[9] | I/O, HS_LVCMOS | M3 DQ[9]. |
| AV3 | M3_DQ[10] | I/O, HS_LVCMOS | M3 DQ[10]. |
| AT3 | M3_DQ[11] | I/O, HS_LVCMOS | M3 DQ[11]. |
| AW7 | M3_DQ[12] | I/O, HS_LVCMOS | M3 DQ[12]. |
| BC3 | M3_DQ[13] | I/O, HS_LVCMOS | M3 DQ[13]. |
| BB2 | M3_DQ[14] | I/O, HS_LVCMOS | M3 DQ[14]. |
| BC2 | M3_DQ[15] | I/O, HS_LVCMOS | M3 DQ[15]. |
| AR11 | M3_DQSp[0] | I/O, HS_LVCMOS | M3 DQSp[0] BYTE0. |
| AW9 | M3_DQSp[1] | I/O, HS_LVCMOS | M3 DQSp[1] BYTE1. |
| AR9 | M3_DQSn[0] | I/O, HS_LVCMOS | M3 DQSn[0] BYTE0. |
| AW11 | M3_DQSn[1] | I/O, HS_LVCMOS | M3 DQSn[1] BYTE1. |

Table 24. LPDDR4 Others

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------|-----------|--|
| N23 | MO_VREF | I, Analog | LPDDR4 VREF (left floating) for M0 DQ DQS. |
| L27 | MO_CAL | I, Analog | LPDDR4 Calibration pad. Connect to VSS via a 120 ohm resistor. |
| AG11 | M2_CAL | I, Analog | LPDDR4 Calibration pad. Connect to VSS via a 120 ohm resistor. |

Table 25. HDMI CEC Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-------------|-------------|---|
| AH60 | SM_HDMI_CEC | I/Ood, CMOS | SM HDMI Consumer Electronics Control signal. This pin is 1.8V-only. |

Table 26. HDMI HPD Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|----------------|----------|--|
| BB60 | SM_HDMI_RX_HPD | O, CMOS | HDMI RX hot plug detect. This pin is used to drive the HPD signal on the HDMI RX (sink) port. This pin is 1.8V-only. |
| AG60 | SM_HDMI_TX_HPD | I, CMOS | HDMI TX (source) hot plug detect. This pin is 1.8V-only. |

Table 27. HDMI Receiver 5V Sense Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------------|----------|--|
| BB61 | SM_HDMI_RX_PWR5V | I, CMOS | HDMI source 5V supply detect. This pin is a 1.8V-only input pin. |

Table 28. Two-Wire Serial SM Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------|-------------|------------------------|
| AF59 | SM_TW2_SCL | I/Ood, CMOS | SM TWSI2 serial clock. |
| AD59 | SM_TW2_SDA | I/Ood, CMOS | SM TWSI2 serial data. |
| AR51 | SM_TW3_SCL | I/Ood, CMOS | SM TWSI3 serial clock. |
| AR53 | SM_TW3_SDA | I/Ood, CMOS | SM TWSI3 serial data. |

Table 29. SoC Two-Wire Serial Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------|-------------|--------------------|
| AC47 | TWO_SCL | I/Ood, CMOS | TWSI serial clock. |
| AC49 | TWO_SDA | I/Ood, CMOS | TWSI serial data. |

Table 30. SoC SPI Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|----------|--|
| H59 | SPI1_SS0n | O, CMOS | SPI1 chip select 0 for first slave device with handler. |
| F59 | SPI1_SS1n | O, CMOS | SPI1 chip select 1 for second slave device with handler. |
| K60 | SPI1_SS2n | O, CMOS | SPI1 chip select 2 for third slave device. |
| H60 | SPI1_SS3n | O, CMOS | SPI1 chip select 3 for fourth slave device. |
| L59 | SPI1_SCLK | O, CMOS | SPI1 serial clock. |
| M59 | SPI1_SDI | I, CMOS | SPI1 serial data input. |
| K61 | SPI1_SDO | O, CMOS | SPI1 serial data output. |

Table 31. PCIe Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------|-----------|---|
| CA22 | PCIE_CLKp | O, Analog | PCIE RefClk positive. |
| BY22 | PCIE_CLKn | O, Analog | PCIE RefClk negative. |
| BL31 | PCIE_REXT | I, Analog | PCIE Reference resistor connection. Connect to VSS via a 200 ohm resistor. |
| BY18 | PCIE_RX0p | I, Analog | PCIE 0 receive positive. |
| BW18 | PCIE_RX0n | I, Analog | PCIE 0 receive negative. |
| BW12 | PCIE_RX1p | I, Analog | PCIE 1 receive positive. |
| BW14 | PCIE_RX1n | I, Analog | PCIE 1 receive negative. |
| BW20 | PCIE_TX0p | O, Analog | PCIE 0 transmit positive. |
| BW19 | PCIE_TX0n | O, Analog | PCIE 0 transmit negative. |
| BY16 | PCIE_TX1p | O, Analog | PCIE 1 transmit positive. |
| CA16 | PCIE_TX1n | O, Analog | PCIE 1 transmit negative. |

Table 32. RGMII Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------|-----------|---------------------------------|
| T60 | RGMII_MDC | O, CMOS | RGMII management data clock. |
| W55 | RGMII_MDIO | I/O, CMOS | RGMII management data. |
| AG49 | RGMII_RXC | I, CMOS | RGMII receive reference clock. |
| AC55 | RGMII_RXCTL | I, CMOS | RGMII receive control input. |
| AC53 | RGMII_RXD[0] | I, CMOS | RGMII receive data 0. |
| AB61 | RGMII_RXD[1] | I, CMOS | RGMII receive data 1. |
| Y60 | RGMII_RXD[2] | I, CMOS | RGMII receive data 2. |
| AG51 | RGMII_RXD[3] | I, CMOS | RGMII receive data 3. |
| T61 | RGMII_TXC | O, CMOS | RGMII transmit reference clock. |
| AC51 | RGMII_TXCTL | O, CMOS | RGMII transmit control output. |
| V59 | RGMII_TXD[0] | O, CMOS | RGMII transmit data 0. |
| AG47 | RGMII_TXD[1] | O, CMOS | RGMII transmit data 1. |
| W59 | RGMII_TXD[2] | O, CMOS | RGMII transmit data 2. |
| Y59 | RGMII_TXD[3] | O, CMOS | RGMII transmit data 3. |

Table 33. eMMC Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------|-----------|-----------------------|
| A54 | EMMC_CLK | O, CMOS | Output clock. |
| C51 | EMMC_RSTn | O, CMOS | Hardware reset. |
| B56 | EMMC_STRB | I, CMOS | eMMC 5.0 data strobe. |
| D59 | EMMC_DATA[0] | I/O, CMOS | Data[0]. |
| C59 | EMMC_DATA[1] | I/O, CMOS | Data[1]. |
| C56 | EMMC_DATA[2] | I/O, CMOS | Data[2]. |
| C61 | EMMC_DATA[3] | I/O, CMOS | Data[3]. |
| C60 | EMMC_DATA[4] | I/O, CMOS | Data[4]. |
| B54 | EMMC_DATA[5] | I/O, CMOS | Data[5]. |
| C50 | EMMC_DATA[6] | I/O, CMOS | Data[6]. |
| C58 | EMMC_DATA[7] | I/O, CMOS | Data[7]. |
| C52 | EMMC_CMD | I/O, CMOS | Command/Response. |

Table 34. SDIO Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------|-----------|--|
| J47 | SDIO_CDn | I, CMOS | Card Detect. 0 = Detect. |
| B48 | SDIO_CLK | O, CMOS | Output clock. CLK in SPI mode. |
| B50 | SDIO_CMD | I/O, CMOS | Command/Response. DO in SPI mode. |
| N43 | SDIO_DATA[0] | I/O, CMOS | DATA[0], busy from card. DI in SPI mode. |
| C44 | SDIO_DATA[1] | I/O, CMOS | Data[1]. Int from card. |
| C46 | SDIO_DATA[2] | I/O, CMOS | Data[2]. Read wait from card. |
| G47 | SDIO_DATA[3] | I/O, CMOS | Data[3]. SSn in SPI mode. |
| L47 | SDIO_WP | I, CMOS | Write Protect. 1= Write-protected. |

Table 35. SM Analog Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|------------|-------------|-----------------------------------|
| BC55 | SM_ADCI[0] | I, Analog | ADC input. Full input range 1.2V. |
| BC53 | SM_ADCI[1] | I, Analog | ADC input. Full input range 1.2V. |
| AW49 | SM_RCLKI | I, Analog | Oscillator/Crystal Input 25 MHz. |
| AW47 | SM_RCLKO | I/O, Analog | Crystal inverted output. |

Table 36. System Manager (SM) Global Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-------------|----------|--|
| AH61 | SM_JTAG_SEL | Id, CMOS | SM JTAG port selection. 1 = Enable SM JTAG. |
| AL49 | SM_POR_EN | Iu, CMOS | Enable on-chip power-on reset (POR_VDD) feature in SM. |
| AL55 | SM_RSTIn | Iu, CMOS | SoC Active low reset input with internal pull-up. |
| AM59 | SM_TCK | Id, CMOS | SM JTAG clock input. |
| AP60 | SM_TDI | Iu, CMOS | SM JTAG SDATA IN. |
| AR60 | SM_TDO | Ou, CMOS | SM JTAG SDATA OUT. |
| AK59 | SM_TEST_EN | Id, CMOS | TEST enable. 1 = Enable scan. 0 = Enable ARM ICE JTAG connections. |
| AP59 | SM_TMS | Iu, CMOS | SM JTAG Mode select signal (ARM or chip JTAG). |
| AL51 | SM_TRSTn | Id, CMOS | SM JTAG reset. |

Table 37. System Manager (SM) SPI Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------------|----------|-----------------------------|
| AV59 | SM_SPI2_SCLK | O, CMOS | SM SPI2 serial clock. |
| AW57 | SM_SPI2_SDI | I, CMOS | SM SPI2 serial data input. |
| AY60 | SM_SPI2_SDO | Od, CMOS | SM SPI2 serial data output. |
| AR61 | SM_SPI2_SS0n | Od, CMOS | SM SPI2 chip select 0. |
| AR55 | SM_SPI2_SS1n | Od, CMOS | SM SPI2 chip select 1. |
| AT59 | SM_SPI2_SS2n | O, CMOS | SM SPI2 chip select 2. |
| AY59 | SM_SPI2_SS3n | O, CMOS | SM SPI2 chip select 3. |

Table 38. SM UART Interface

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-------------|----------|-------------|
| AW51 | SM_URTO_RXD | I, CMOS | UART0 RX. |
| AW55 | SM_URTO_TXD | Od, CMOS | UART0 TX. |
| AB60 | SM_URT1_RXD | I, CMOS | UART1 RX. |
| AG59 | SM_URT1_TXD | O, CMOS | UART1 TX. |

Table 39. MIPI Camera Serial Interface (CSIO) Pins

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|----------------|-----------|---|
| BC7 | MIPI_CSIO_ATB | I, Analog | MIPI CSIO Analog test pin. |
| BP1 | MIPI_CSIO_CKp | I, Analog | MIPI CSIO CLK positive. |
| BP2 | MIPI_CSIO_CKn | I, Analog | MIPI CSIO CLK negative. |
| BM3 | MIPI_CSIO_D0p | I, Analog | MIPI CSIO Data Lane 0 positive. |
| BL3 | MIPI_CSIO_D0n | I, Analog | MIPI CSIO Data Lane 0 negative. |
| BK2 | MIPI_CSIO_D1p | I, Analog | MIPI CSIO Data Lane 1 positive. |
| BK3 | MIPI_CSIO_D1n | I, Analog | MIPI CSIO Data Lane 1 negative. |
| BF3 | MIPI_CSIO_D2p | I, Analog | MIPI CSIO Data Lane 2 positive. |
| BD3 | MIPI_CSIO_D2n | I, Analog | MIPI CSIO Data Lane 2 negative. |
| BH2 | MIPI_CSIO_D3p | I, Analog | MIPI CSIO Data Lane 3 positive. |
| BH1 | MIPI_CSIO_D3n | I, Analog | MIPI CSIO Data Lane 3 negative. |
| BC9 | MIPI_CSIO_REXT | I, Analog | MIPI CSIO reference resistor connection. Connect to VSS via a 200 ohm resistor. |

Table 40. MIPI Camera Serial Interface (CSI1) Pins

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|----------------|-----------|--|
| CA3 | MIPI_CSI1_CKp | I, Analog | MIPI CSI1 CLK positive. |
| BY3 | MIPI_CSI1_CKn | I, Analog | MIPI CSI1 CLK negative. |
| BT2 | MIPI_CSI1_D0p | I, Analog | MIPI CSI1 Data Lane 0 positive. |
| BT3 | MIPI_CSI1_D0n | I, Analog | MIPI CSI1 Data Lane 0 negative. |
| BW3 | MIPI_CSI1_D1p | I, Analog | MIPI CSI1 Data Lane 1 positive. |
| BV3 | MIPI_CSI1_D1n | I, Analog | MIPI CSI1 Data Lane 1 negative. |
| BG9 | MIPI_CSI1_REXT | I, Analog | MIPI CSI1 reference resistor connection. Connect to VSS via a 200 ohm resistor. |

Table 41. MIPI Display Serial Interface Pins

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|---------------|-----------|---|
| BN35 | MIPI_DSI_ATB | O, Analog | MIPI DSI Analog test output. |
| CA28 | MIPI_DSI_CKp | O, Analog | MIPI DSI CLK positive. |
| BY28 | MIPI_DSI_CKn | O, Analog | MIPI DSI CLK negative. |
| BW24 | MIPI_DSI_D0p | O, Analog | MIPI DSI Data Lane 0 positive. |
| BY24 | MIPI_DSI_D0n | O, Analog | MIPI DSI Data Lane 0 negative. |
| BW27 | MIPI_DSI_D1p | O, Analog | MIPI DSI Data Lane 1 positive. |
| BW26 | MIPI_DSI_D1n | O, Analog | MIPI DSI Data Lane 1 negative. |
| BW32 | MIPI_DSI_D2p | O, Analog | MIPI DSI Data Lane 2 positive. |
| BW34 | MIPI_DSI_D2n | O, Analog | MIPI DSI Data Lane 2 negative. |
| BW30 | MIPI_DSI_D3p | O, Analog | MIPI DSI Data Lane 3 positive. |
| BY30 | MIPI_DSI_D3n | O, Analog | MIPI DSI Data Lane 3 negative. |
| BL35 | MIPI_DSI_REXT | O, Analog | MIPI DSI reference resistor connection. Connect to VSS via a 200 ohm resistor. |

Table 42. Power - 1.8V

| Pin Location(s) | Signal | Pin Type | Description |
|-------------------------|----------------------|----------|----------------------------------|
| BR55 | AVPLL_AVDD1P8 | PWR | 1.8V AVPLL analog power. |
| J51 | CPULL_AVDD1P8 | PWR | 1.8V CPULL analog power. |
| R47 | CPUTSEN_AVDD1P8 | PWR | 1.8V CPUTSEN analog power. |
| E51 | EMMC_VDDIO1P8 | PWR | 1.8V EMMC power. |
| BN47 | HDMI_RX_AVDD1P8 | PWR | 1.8V HDMI RX supply. |
| BU57 | HDMI_TX_AVDD1P8 | PWR | 1.8V HDMI TX supply. |
| BN51 | HDMI_TX_HEAC_AVDD1P8 | PWR | 1.8V HDMI TX HEAC supply. |
| BD16 | KILOOTP_AVDD1P8 | PWR | 1.8V AVDD KILO OTP analog power. |
| J43 | MEMPLL_AVDD1P8 | PWR | 1.8V memPLL analog power. |
| BG5 | MIPI_CSIO_AVDD1P8 | PWR | 1.8V MIPI CSIO analog power. |
| BL7 | MIPI_CSI1_AVDD1P8 | PWR | 1.8V MIPI CSI1 analog power. |
| BU39 | MIPI_DSI_AVDD1P8 | PWR | 1.8V MIPI DSI analog power. |
| AD19 | M0_AVDD1P8 | PWR | 1.8V M0 analog power. |
| BU27 | PCIE_AVDD1P8 | PWR | 1.8V PCIe analog power. |
| BR27 | PCIE_PLL_AVDD1P8 | PWR | 1.8V PCIe PLL analog power. |
| G43 | SDIO_VDDIO1P8 | PWR | 1.8V SDIO analog power. |
| BC51 | SM_ADC_AVDD1P8 | PWR | 1.8V SM ADC analog power. |
| BC57 | SM_OSC_VDDIO1P8 | PWR | 1.8V SM OSC analog power. |
| BC47 | SM_TSEN_AVDD1P8 | PWR | 1.8V SM TSEN analog power. |
| AL47 | SM_VDDIO1P8 | PWR | 1.8V SM digital I/O power. |
| BG49 | SYSPLL_AVDD1P8 | PWR | 1.8V SYSPLL analog power. |
| BL55, BL57, L53, L55 | VDDIO1P8 | PWR | 1.8V SoC digital I/O power. |

Table 43. Power - 3.3V

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|-----------------|----------|------------------------------|
| BR47 | HDMI_RX_AVDD3P3 | PWR | 3.3V HDMI RX supply. |
| A48 | SDIO_VDDIO3P3 | PWR | 3.3V SDIO digital I/O power. |
| BR7 | USB2_AVDD3P3 | PWR | 3.3V USB2.0 analog power. |
| BU7 | USB2_VR_AVDD3P3 | PWR | 3.3V USB2.0 VR analog power. |
| BR11 | USB3_AVDD3P3 | PWR | 3.3V USB3.0 analog power. |

Table 44. Power and Ground Pins (Sheet 1 of 3)

| Pin Location(s) | Signal | Pin Type | Description |
|---|-------------------|----------|--------------------------------------|
| BN55 | AVPLL_AVSS | GND | AVPLL analog ground. |
| L51 | CPUPLL_AVSS | GND | CPUPLL analog ground. |
| T44 | CPUTSEN_AVSS | GND | CPUTSEN analog ground. |
| BU51 | HDMI_RX_AVDD | PWR | HDMI RX analog power. |
| BN43 | HDMI_RX_DVDD | PWR | HDMI RX digital power. |
| BW51 | HDMI_TX_AVDD | PWR | HDMI TX analog power. |
| BJ47 | HDMI_TX_HEAC_AVDD | PWR | HDMI TX HEAC analog power. |
| L43 | MEMPLL_AVSS | GND | MEMPLL analog ground. |
| BC11 | MIPI_CSIO_AVDD | PWR | MIPI CSIO analog power. |
| BG13 | MIPI_CSI1_AVDD | PWR | MIPI CSI1 analog power. |
| BR35 | MIPI_DSI_AVDD | PWR | MIPI DSI analog power. |
| BU15 | PCIE_AVDD | PWR | PCie analog power. |
| BN27 | PCIE_PLL_AVSS | GND | PCie PLL analog ground. |
| BR31 | PCIE_REFCLK_AVDD | PWR | PCie REFCLK analog power. |
| BR23 | PCIE_TX_AVDD[0] | PWR | PCie TX analog power. |
| BR19 | PCIE_TX_AVDD[1] | PWR | PCie TX analog power. |
| BC49 | SM_ADC_AVSS | GND | SM ADC analog ground. |
| BB44 | SM_TSEN_AVSS | GND | SM temperature sensor analog ground. |
| AR47 | SM_VDD_CORE | PWR | SM digital core power. |
| BG47 | SYSPLL_AVSS | GND | SYSPLL analog ground. |
| BN11 | USB2_DVDD | PWR | USB 2.0 digital core power. |
| BL15 | USB3_AVDD | PWR | USB 3.0 PHY analog power. |
| BR15 | USB3_DVDD | PWR | USB 3.0 PHY digital power. |
| AG26, AG32, AK26, AK32, AM26, AM32, AM38, AM44, AR22, AR28, AR35, AR42, AV19, AV26, AV32, AV38, AV44, BB16, BB22, BB28, BB35, BB42, BD19, BD26, BD32, BD38, BD44, BF18, BJ19, BJ27, BJ35 | VDD_CORE | PWR | SoC core power. |

Table 44. Power and Ground Pins (Sheet 2 of 3)

| Pin Location(s) | Signal | Pin Type | Description |
|--|-------------|----------|--|
| AG57 | VDD_CORE_FB | PWR | Core voltage feedback compensation. |
| AD32, AD38, AD44, AG35, AG42, AK38, AK44, V32, V38, Y35, Y42 | VDD_CPU | PWR | SoC CPU power. |
| AG55 | VDD_CPU_FB | PWR | CPU voltage feedback compensation. |
| AG13, AK19, AM19, AR16, AR18, N15, N19, N27, V16, W13, Y22, Y28, Y30 | VDDQ | PWR | LPDDR4 I/O power 1.1V. |
| AD26, AD28, AF19, AG19, AR19, AT19, Y19, Y26 | VDDQLP | PWR | LPDDR4 I/O power 1.1V or LPDDR4x I/O power 0.6V. |
| A1, A2, A60, A61, AB3, AB59, AC5, AC57, AD16, AD22, AD35, AD42, AG16, AG22, AG28, AG34, AG38, AG44, AG53, AG9, AH3, AH59, AK16, AK22, AK28, AK35, AK42, AL5, AL53, AL57, AM16, AM22, AM28, AM35, AM42, AR13, AR26, AR27, AR3, AR32, AR38, AR40, AR44, AR49, AR5, AR57, AR59, AV16, AV22, AV28, AV35, AV42, AW13, AW53, B1, B2, B60, B61, BB19, BB26, BB3, BB32, BB38, BB59, BC13, BC5, BC59, BD22, BD28, BD35, BD42, BG11, | VSS | GND | Ground. |

Table 44. Power and Ground Pins (Sheet 3 of 3)

| Pin Location(s) | Signal | Pin Type | Description |
|--|-----------------------|----------|-------------|
| BG51, BG57, BG7, BH3, BH59, BJ15, BJ23, BJ31, BJ39, BL19, BL47, BL5, BL53, BN15, BN19, BN31, BN39, BP3, BP59, BR5, BR51, BR57, BU11, BU19, BU23, BU31, BU35, BU43, BU47, BU55, BW10, BW16, BW22, BW28, BW35, BW42, BW48, BY1, BY2, BY60, BY61, C10, C16, C22, C28, C35, C42, C48, C54, CA1, CA2, CA60, CA61, E11, E19, E23, E31, E35, E43, E47, E55, E7, G15, G5, G51, G57, J11, K3, K59, L11, L5, L57, L9, N13, N35, N47, N49, T3, T59, V19, V22, V26, V28, V35, V42, V44, W5, W51, W57, Y16, Y32, Y34, Y38, Y44 | VSS (continued...) | GND | Ground. |

Table 45. Not Connected

| Pin Location(s) | Signal | Pin Type | Description |
|-----------------|--------|----------|----------------|
| BR39 | NC | NC | Not connected. |
| BR43 | NC | NC | Not connected. |
| BY35 | NC | NC | Not connected. |
| CA35 | NC | NC | Not connected. |

2. Pin Multiplexing

2.1. Pin Multiplexing Signal Descriptions

For complete pin multiplexing details, refer to [Section 2.2., Pin Multiplexing Modes](#).

Note: The Pin Type in the tables in this section only represents the signal direction of the multiplexed signal. For other pin properties, such as open drain or pull-up, refer to the corresponding primary pin in the pin description table (see [Section 1.2., Pin Descriptions](#)).

Table 46. Audio MIC PDM

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|-----------|---------------------|
| BP60 | PDMA_CLKIO | I/O, CMOS | PDM A Clock In/Out. |
| BT60 | PDMA_DI[0] | I, CMOS | PDM A Data in. |
| BT61 | PDMA_DI[1] | I, CMOS | PDM A Data in. |
| BM59 | PDMA_DI[2] | I, CMOS | PDM A Data in. |
| BT59 | PDMA_DI[3] | I, CMOS | PDM A Data in. |
| BH61 | PDMA_DI[2] | I, CMOS | PDM B Data in. |
| BF59 | PDMA_DI[3] | I, CMOS | PDM B Data in. |
| BP61 | PDMA_CLKIO | I/O, CMOS | PDM B Clock In/Out. |
| BL59 | PDMC_DI[0] | I, CMOS | PDM C Data in. |

Note: PDMA, PDMA, and PDMC are alternative pin locations for the same PDM interface.

Table 47. General Purpose I/O Interface (Sheet 1 of 3)

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|-----------|----------------------|
| CA59 | GPIO[0] | I/O, CMOS | General purpose I/O. |
| BY59 | GPIO[1] | I/O, CMOS | General purpose I/O. |
| CA58 | GPIO[2] | I/O, CMOS | General purpose I/O. |
| BV59 | GPIO[3] | I/O, CMOS | General purpose I/O. |
| BL59 | GPIO[4] | I/O, CMOS | General purpose I/O. |
| BL51 | GPIO[5] | I/O, CMOS | General purpose I/O. |
| BL49 | GPIO[6] | I/O, CMOS | General purpose I/O. |
| BP61 | GPIO[7] | I/O, CMOS | General purpose I/O. |
| BT60 | GPIO[8] | I/O, CMOS | General purpose I/O. |
| BT61 | GPIO[9] | I/O, CMOS | General purpose I/O. |
| BM59 | GPIO[10] | I/O, CMOS | General purpose I/O. |
| BT59 | GPIO[11] | I/O, CMOS | General purpose I/O. |
| BP60 | GPIO[12] | I/O, CMOS | General purpose I/O. |
| BM60 | GPIO[13] | I/O, CMOS | General purpose I/O. |
| BK59 | GPIO[14] | I/O, CMOS | General purpose I/O. |
| BF59 | GPIO[15] | I/O, CMOS | General purpose I/O. |

Table 47. General Purpose I/O Interface (Sheet 2 of 3)

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|-----------------------|-----------|--|
| BH61 | GPIO[16] | I/O, CMOS | General purpose I/O. |
| BF60 | GPIO[17] | I/O, CMOS | General purpose I/O. |
| BG53 | GPIO[18] | I/O, CMOS | General purpose I/O. |
| BD59 | GPIO[19] | I/O, CMOS | General purpose I/O. |
| BH60 | GPIO[20] | I/O, CMOS | General purpose I/O. |
| BG55 | GPIO[21] | I/O, CMOS | General purpose I/O. |
| AC51 | GPIO[22] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| T61 | GPIO[23] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| Y59 | GPIO[24] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| W59 | GPIO[25] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| AG47 | GPIO[26] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| V59 | GPIO[27] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| W55 | GPIO[28] | I/O, CMOS | General purpose I/O. |
| T60 | GPIO[29] | I/O, CMOS | General purpose I/O. |
| AC55 | GPIO[30] | I/O, CMOS | General purpose I/O. |
| AG49 | GPIO[31] | I/O, CMOS | General purpose I/O. |
| AG51 | GPIO[32] | I/O, CMOS | General purpose I/O. |
| Y60 | GPIO[33] | I/O, CMOS | General purpose I/O. |
| AB61 | GPIO[34] | I/O, CMOS | General purpose I/O. |
| AC53 | GPIO[35] | I/O, CMOS | General purpose I/O. |
| P60 | GPIO[36] | I/O, CMOS | General purpose I/O. |
| P59 | GPIO[37] | I/O, CMOS | General purpose I/O. |
| R55 | GPIO[38] | I/O, CMOS | General purpose I/O. |
| R57 | GPIO[39] | I/O, CMOS | General purpose I/O. |
| R53 | GPIO[40] | I/O, CMOS | General purpose I/O. |
| W49 | GPIO[41] | I/O, CMOS | General purpose I/O. |
| R51 | GPIO[42] | I/O, CMOS | General purpose I/O. |
| W47 | GPIO[43] | I/O, CMOS | General purpose I/O. |
| L47 | GPIO[44] | I/O, CMOS | General purpose I/O. |
| J47 | GPIO[45] | I/O, CMOS | General purpose I/O. |
| AC49 | GPIO[46] | I/O, CMOS | General purpose I/O. |
| AC47 | GPIO[47] | I/O, CMOS | General purpose I/O. |
| M59 | GPIO[48] | I/O, CMOS | General purpose I/O. |
| L59 | GPIO[49] | I/O, CMOS | General purpose I/O. |
| K61 | GPIO[50] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| H60 | GPIO[51] | I/O, CMOS | General purpose I/O. |
| K60 | GPIO[52] | I/O, CMOS | General purpose I/O. |

Table 47. General Purpose I/O Interface (Sheet 3 of 3)

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|-----------------------|-----------|--|
| F59 | GPIO[53] | I/O, CMOS | General purpose I/O. |
| H59 | GPIO[54] ¹ | I/O, CMOS | General purpose I/O. Recommended as output only. |
| W53 | GPIO[55] | I/O, CMOS | General purpose I/O. |

1. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 48. PWM Alternate Interfaces

| Pin # | Pin Mux Name | Pin Type | Description |
|------------------------------------|--------------|----------|---------------------------------------|
| AP59 AT59 K60 R57 BG55 | PWM[0] | O, CMOS | Pulse-Width Modulation output data 0. |
| AP60 AY59 F59 R55 BH60 | PWM[1] | O, CMOS | Pulse-Width Modulation output data 1. |
| AG59 AR51 P59 BH61 | PWM[2] | O, CMOS | Pulse-Width Modulation output data 2. |
| AB60 AR53 P60 BF59 | PWM[3] | O, CMOS | Pulse-Width Modulation output data 3. |

Table 49. SM Global Interface

| Pin # | Pin Mux Name | Pin Type | Description |
|--------------|--------------------------|---|---|
| AB60 AT59 | CLK_25M | O, CMOS | 25MHz digital clock output for system usage like RGMII PHY. |
| AF59 | RX_EDID_SCL | I/Ood, CMOS | HDMIRX EDDC SCL |
| AD59 | RX_EDID_SDA | I/Ood, CMOS | HDMIRX EDDC SDA |
| AF59 | SM_GPIO[0] | I/O, CMOS | SM GPIO (Interrupt, remote, and so on). |
| AD59 | SM_GPIO[1] | | SM GPIO (Interrupt, remote, and so on). |
| AG60 | SM_GPIO[2] | | SM GPIO (Interrupt, remote, and so on). |
| AH60 | SM_GPIO[3] | | SM GPIO (Interrupt, remote, and so on). |
| AG59 | SM_GPIO[4] | | SM GPIO (Interrupt, remote, and so on). |
| AB60 | SM_GPIO[5] | | SM GPIO (Interrupt, remote, and so on). |
| AP59 | SM_GPIO[6] | | SM GPIO (Interrupt, remote, and so on). |
| AP60 | SM_GPIO[7] | | SM GPIO (Interrupt, remote, and so on). |
| AR60 | SM_GPIO[8] ¹ | | SM GPIO (Interrupt, remote, and so on). Recommended as output only. |
| AR51 | SM_GPIO[9] | | SM GPIO (Interrupt, remote, and so on). |
| AR53 | SM_GPIO[10] | | SM GPIO (Interrupt, remote, and so on). |
| AV59 | SM_GPIO[11] | | SM GPIO (Interrupt, remote, and so on). |
| AW57 | SM_GPIO[12] | | SM GPIO (Interrupt, remote, and so on). |
| AY60 | SM_GPIO[13] ¹ | | SM GPIO (Interrupt, remote, and so on). Recommended as output only. |
| AY59 | SM_GPIO[14] | | SM GPIO (Interrupt, remote, and so on). |
| AT59 | SM_GPIO[15] | | SM GPIO (Interrupt, remote, and so on). |
| AR55 | SM_GPIO[16] ¹ | | SM GPIO (Interrupt, remote, and so on). Recommended as output only. |
| AR61 | SM_GPIO[17] ¹ | | SM GPIO (Interrupt, remote, and so on). Recommended as output only. |
| AW51 | SM_GPIO[18] | | SM GPIO (Interrupt, remote, and so on). |
| AW55 | SM_GPIO[19] ¹ | | SM GPIO (Interrupt, remote, and so on). Recommended as output only. |
| BB60 | SM_GPIO[20] | | SM GPIO (Interrupt, remote, and so on). |
| BB61 | SM_GPIO[21] | SM GPIO (Interrupt, remote, and so on). | |
| AY59 | SM_PWR_OK | I, CMOS | Power Good Detect input. |
| AG59 AT59 | SM_TIMER[0] | O, CMOS | SM Timer output. |
| AB60 AY59 | SM_TIMER[1] | O, CMOS | SM Timer output. |
| AF59 | SM_TW2A_SCL | I/Ood, CMOS | TWSI 2A serial clock. |
| AD59 | SM_TW2A_SDA | I/Ood, CMOS | TWSI 2A serial data. |
| AG59 | SM_TW2B_SCL | I/Ood, CMOS | TWSI 2B serial clock. |

Table 49. SM Global Interface (Continued)

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|---------------|-------------|----------------------|
| AB60 | SM_TW2B_SDA | I/Ood, CMOS | TWSI 2B serial data. |
| AY59 | SM_UART1_CTSn | I, CMOS | SM UART1 CTSn. |
| AR55 | SM_UART1_RTSn | O, CMOS | SM UART1 RTSn. |
| AW57 | URT2_CTSn | I, CMOS | UART2 CTSn. |
| AY60 | URT2_RTSn | O, CMOS | UART2 RTSn. |
| AY59 | URT2_RXD | I, CMOS | UART2 RXD. |
| AT59 | URT2_TXD | O, CMOS | UART2 TXD. |

1. Recommended as output only. When used as input, the external driving source shall not interfere with the pin's strap mode or mode 0 function.

Table 50. Serial Transport Interface

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|----------|--------------------------------------|
| BF60 | STS2_CLK | I, CMOS | Serial TS capture serial data clock. |
| BH61 | STS2_SD | I, CMOS | Serial TS capture serial data. |
| BF59 | STS2_VALD | I, CMOS | Serial TS capture valid flag. |
| BG53 | STS2_SOP | I, CMOS | Serial TS capture start of packet. |
| BV59 | STS3_CLK | I, CMOS | Serial TS capture serial data clock. |
| CA58 | STS3_SD | I, CMOS | Serial TS capture serial data. |
| CA59 | STS3_VALD | I, CMOS | Serial TS capture valid flag. |
| BY59 | STS3_SOP | I, CMOS | Serial TS capture start of packet. |
| BT61 | STS4_CLK | I, CMOS | Serial TS capture serial data clock. |
| BT60 | STS4_SD | I, CMOS | Serial TS capture serial data. |
| BM59 | STS4_VALD | I, CMOS | Serial TS capture valid flag. |
| R51 | STS5_CLK | I, CMOS | Serial TS capture serial data clock. |
| R53 | STS5_SD | I, CMOS | Serial TS capture serial data. |
| R55 | STS6_CLK | I, CMOS | Serial TS capture serial data clock. |
| P60 | STS6_SD | I, CMOS | Serial TS capture serial data. |
| K60 | STS7_CLK | I, CMOS | Serial TS capture serial data clock. |
| H60 | STS7_SD | I, CMOS | Serial TS capture serial data. |
| F59 | STS7_VALD | I, CMOS | Serial TS capture valid flag. |

Table 51. SoC Reset Strapping

| Pin # | Pin Mux Name | Primary Pin Name | Pin Type | Description |
|-------|------------------------------|------------------|----------|---|
| BK59 | boot_src[1] | SPDIFO | PU-boot | CPU Boot Source bit[1] |
| BP61 | boot_src[0] | I2S2_MCLK | PD-boot | CPU boot source bit[0]. boot_src[1:0]: 00: ROM boot from SPI 01: Reserved 10: ROM boot from EMMC 11: Direct boot from SPI (Reserved for factory use only) |
| K61 | software_strap[0](USB_BOOTn) | SPI1_SDO | PU-boot | Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB 1: Boot from the device selected by boot_src |
| H59 | software_strap[1] | SPI1_SS0n | PD-boot | Straps for software usage |
| T61 | legacy_boot | RGMII_TXC | PD-boot | Strap to reduce reset wait time 0: 2ms 1: 20ms |
| V59 | software_strap[2] | RGMII_TXD[0] | PD-boot | Straps for software usage |
| AG47 | software_strap[3] | RGMII_TXD[1] | PD-boot | Straps for software usage |
| W59 | cpuRstByps | RGMII_TXD[2] | PD-boot | CPU reset bypass strap 0: Enable reset logic inside cpu partition 1: Bypass reset logic inside cpu partition |
| Y59 | pllPwrDown | RGMII_TXD[3] | PD-boot | SYS/MEM/CPU PLL Power Down 1: Power Down 0: Power UP |
| AC51 | pllByps | RGMII_TXCTL | PD-boot | SYS/MEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed |
| AW55 | SM_STRP[0] | SM_URTO_TXD | PD-boot | SM to SOC RSTn mode select 0: Releasing of the SoC reset does not wait for SM_PWR_OK(mode_0 of SM_SPI2_SS3n, system will assert this signal when SOC core power is ready). 1: Releasing of the SoC reset waits for SM_PWR_OK. |
| AY60 | SM_STRP[1] | SM_SPI2_SDO | PD-boot | Software strap. |
| AR61 | SM_STRP[2] | SM_SPI2_SS0n | PD-boot | Software strap. |
| AR55 | SM_STRP[3] | SM_SPI2_SS1n | PD-boot | Software strap. |

Table 52. SoC TWSI Interface

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|-------------|--------------------|
| J47 | TW1A_SCL | I/Ood, CMOS | TW1A serial clock. |
| L47 | TW1A_SDA | I/Ood, CMOS | TW1A serial data. |
| K60 | TW1B_SCL | I/Ood, CMOS | TW1B serial clock. |
| H60 | TW1B_SDA | I/Ood, CMOS | TW1B serial data. |

Table 53. SoC UART Interface

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|----------|-------------|
| W49 | URT3_CTSn | I, CMOS | UART3 CTSn. |
| R53 | URT3_RTSn | O, CMOS | UART3 RTSn. |
| W47 | URT3_RXD | I, CMOS | UART3 RXD. |
| R51 | URT3_TXD | O, CMOS | UART3 TXD. |

Table 54. PHY Debug Interface

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|--------------|----------|---------------------------|
| W47 | PHY_DBG[0] | O, CMOS | PHY Debug output data 0. |
| R51 | PHY_DBG[1] | O, CMOS | PHY Debug output data 1. |
| W49 | PHY_DBG[2] | O, CMOS | PHY Debug output data 2. |
| R53 | PHY_DBG[3] | O, CMOS | PHY Debug output data 3. |
| R57 | PHY_DBG[4] | O, CMOS | PHY Debug output data 4. |
| R55 | PHY_DBG[5] | O, CMOS | PHY Debug output data 5. |
| P59 | PHY_DBG[6] | O, CMOS | PHY Debug output data 6. |
| P60 | PHY_DBG[7] | O, CMOS | PHY Debug output data 7. |
| T60 | PHY_DBG[8] | O, CMOS | PHY Debug output data 8. |
| W55 | PHY_DBG[9] | O, CMOS | PHY Debug output data 9. |
| AC47 | PHY_DBG[10] | O, CMOS | PHY Debug output data 10. |
| AC49 | PHY_DBG[11] | O, CMOS | PHY Debug output data 11. |
| K60 | PHY_DBG[12] | O, CMOS | PHY Debug output data 12. |
| H60 | PHY_DBG[13] | O, CMOS | PHY Debug output data 13. |
| F59 | PHY_DBG[14] | O, CMOS | PHY Debug output data 14. |
| AG47 | PHY_DBG[15] | O, CMOS | PHY Debug output data 15. |
| L59 | DBG_CLK | O, CMOS | Debug clock. |

Table 55. Test/Monitor Interfaces

| Pin # | Pin Mux Name | Pin Type | Description |
|-------|-----------------|----------|--|
| BG55 | ARC_TEST_OUT | O, CMOS | ARC test output. |
| BK59 | AVPLL_CLKO | O, CMOS | AVPLL monitor output. |
| W47 | CPUPLL_CLKO | O, CMOS | CPU PLL monitor output. |
| BP61 | HDMI_FBCLK | O, CMOS | HDMI CLK feedback. |
| W49 | MEMPLL_CLKO | O, CMOS | MEM PLL monitor output. |
| AT59 | MON_VDD1P8_OUT | O, CMOS | VDD1.8V monitor output. |
| AG59 | PORB_AVDD_LV | O, CMOS | Power on reset for AVDD 1.8V power. |
| AR61 | PORB_AVDD33_LV | O, CMOS | Power on reset for AVDD 3.3V power. |
| AG59 | POR_B_VOUT | O, CMOS | Combined power on reset for VDD, 1.8V, 3.3V power. |
| AB60 | POR_VDDSOC_RSTB | O, CMOS | Power on reset for SoC VDD power. |
| R51 | SYSPLL_CLKO | O, CMOS | SYS PLL monitor output. |
| AR55 | VDD_CPU_PORB | O, CMOS | Power on reset for VDD CPU power. |

2.2. Pin Multiplexing Modes

This section describes the various modes related to the multiplexed pins. The primary pin name reflects the pinout name, while the Mode 0, Mode 1, ..., Mode 7 and Strap multiplex names are located in the respective columns.

Figure 2 shows the multiplexed pin naming scheme that is used for the SM Multiplexed pins.

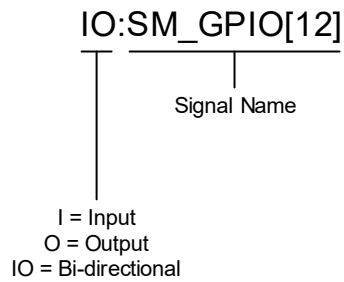


Figure 2. Example of the SM Multiplexed Pin Naming Scheme

Table 56. SM Group Multiplexing

| Ball # | Primary Pin Name | Mode 0 ¹ | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 5 | Mode 6 | Mode 7 | Mode Strap |
|--------|------------------|---------------------------------|---------------------------------|--------------------------|-----------------------|---------------|-------------------------|----------------|------------------|------------|
| AF59 | SM_TW2_SCL | IO:RX_EDID_SCL | IO:SM_TW2A_SCL | IO:SM_GPIO[0] | — | — | — | — | — | — |
| AD59 | SM_TW2_SDA | IO:RX_EDID_SDA | IO:SM_TW2A_SDA | IO:SM_GPIO[1] | — | — | — | — | — | — |
| AG59 | SM_URT1_TXD | O:POR_B_VOUT | O:SM_URT1_TXD | IO:SM_GPIO[4] | O:PWM[2] ² | O:SM_TIMER[0] | O:PORB_AVDD_LV | IO:SM_TW2B_SCL | — | — |
| AB60 | SM_URT1_RXD | IO:SM_GPIO[5] | I:SM_URT1_RXD | O:CLK_25M | O:PWM[3] ² | O:SM_TIMER[1] | O:POR_VDDSOC_RSTB | IO:SM_TW2B_SDA | — | — |
| AG60 | SM_HDMI_TX_HPD | IO:SM_GPIO[2] | I:SM_HDMI_TX_HPD | — | — | — | — | — | — | — |
| AH60 | SM_HDMI_CEC | IO:SM_GPIO[3] | IO:SM_HDMI_CEC | — | — | — | — | — | — | — |
| AP59 | SM_TMS | I:SM_TMS | IO:SM_GPIO[6] | O:PWM[0] ² | — | — | — | — | — | — |
| AP60 | SM_TDI | I:SM_TDI | IO:SM_GPIO[7] | O:PWM[1] ² | — | — | — | — | — | — |
| AR60 | SM_TDO | O:SM_TDO | IO:SM_GPIO[8] (Output Only) | — | — | — | — | — | — | — |
| AR51 | SM_TW3_SCL | IO:SM_GPIO[9] | IO:SM_TW3_SCL | O:PWM[2] ² | — | — | — | — | — | — |
| AR53 | SM_TW3_SDA | IO:SM_GPIO[10] | IO:SM_TW3_SDA | O:PWM[3] ² | — | — | — | — | — | — |
| AR61 | SM_SPI2_SS0n | O:SM_SPI2_SS0n | IO:SM_GPIO[17] (Output Only) | — | — | — | — | — | O:PORB_AVDD33_LV | SM_STRP[2] |
| AR55 | SM_SPI2_SS1n | IO:SM_GPIO[16] (Output Only) | O:SM_SPI2_SS1n | — | — | — | — | O:SM_URT1_RTSn | O:VDD_CPU_PORB | SM_STRP[3] |
| AT59 | SM_SPI2_SS2n | O:MON_VDD1P8_OUT | O:SM_SPI2_SS2n | IO:SM_GPIO[15] | O:PWM[0] ² | O:SM_TIMER[0] | O:URT2_TXD ² | — | O:CLK_25M | — |
| AY59 | SM_SPI2_SS3n | I:SM_PWR_OK | O:SM_SPI2_SS3n | IO:SM_GPIO[14] | O:PWM[1] ² | O:SM_TIMER[1] | I:URT2_RXD ² | — | I:SM_URT1_CTSn | — |
| AY60 | SM_SPI2_SDO | O:SM_SPI2_SDO | IO:SM_GPIO[13] (Output Only) | O:URT2_RTSn ² | — | — | — | — | — | SM_STRP[1] |
| AW57 | SM_SPI2_SDI | I:SM_SPI2_SDI | IO:SM_GPIO[12] | I:URT2_CTSn ² | — | — | — | — | — | — |
| AV59 | SM_SPI2_SCLK | O:SM_SPI2_SCLK | IO:SM_GPIO[11] | — | — | — | — | — | — | — |
| AW55 | SM_URTO_TXD | O:SM_URTO_TXD | IO:SM_GPIO[19] (Output Only) | — | — | — | — | — | — | SM_STRP[0] |
| AW51 | SM_URTO_RXD | I:SM_URTO_RXD | IO:SM_GPIO[18] | — | — | — | — | — | — | — |
| BB60 | SM_HDMI_RX_HPD | O:SM_HDMI_RX_HPD | IO:SM_GPIO[20] | — | — | — | — | — | — | — |
| BB61 | SM_HDMI_RX_PWR5V | I:SM_HDMI_RX_PWR5V | IO:SM_GPIO[21] | — | — | — | — | — | — | — |

1. Mode 0 is the default mode after reset. Strap mode is used only during power-up reset.
2. Function is not available if SoC domain is powered down.

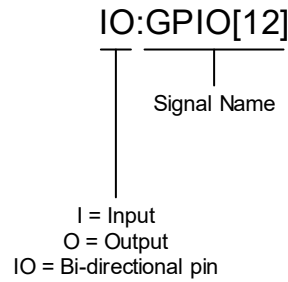


Figure 3. Example of the SoC Multiplexed Pin Naming Scheme

Table 57. SPI Interface Group Multiplexing

| Ball # | Primary Pin Name | Mode 0 ¹ | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 7 | Mode Strap |
|--------|------------------|---------------------|--------------------------|-------------|-------------|----------|---------------|-------------------|
| J47 | SDIO_CDn | IO:SDIO_CDn | IO:GPIO[45] | IO:TW1A_SCL | — | — | — | — |
| L47 | SDIO_WP | IO:SDIO_WP | IO:GPIO[44] | IO:TW1A_SDA | — | — | — | — |
| H59 | SPI1_SS0n | O:SPI1_SS0n | IO:GPIO[54](output only) | — | — | — | — | software_strap[1] |
| F59 | SPI1_SS1n | IO:GPIO[53] | O:SPI1_SS1n | I:STS7_VALD | — | O:PWM[1] | O:PHY_DBG[14] | — |
| K60 | SPI1_SS2n | IO:GPIO[52] | O:SPI1_SS2n | I:STS7_CLK | IO:TW1B_SCL | O:PWM[0] | O:PHY_DBG[12] | — |
| H60 | SPI1_SS3n | IO:GPIO[51] | O:SPI1_SS3n | I:STS7_SD | IO:TW1B_SDA | — | O:PHY_DBG[13] | — |
| K61 | SPI1_SDO | O:SPI1_SDO | IO:GPIO[50](output only) | — | — | — | — | software_strap[0] |
| L59 | SPI1_SCLK | O:SPI1_SCLK | IO:GPIO[49] | — | — | — | O:DBG_CLK | — |
| M59 | SPI1_SDI | I:SPI1_SDI | IO:GPIO[48] | — | — | — | — | — |

1. Mode 0 is the default mode after reset. Strap mode is used only during power-up reset.

Figure 3 shows the multiplexed pin naming scheme that is used for the SoC Multiplexed pins.

Table 58. STSI Group Multiplexing

| Ball # | Primary Pin Name | Mode 0 ¹ | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 7 |
|--------|------------------|---------------------|-------------|---------------|------------|-------------|---------------|
| AC47 | TWO_SCL | IO:GPIO[47] | IO:TWO_SCL | — | — | — | O:PHY_DBG[10] |
| AC49 | TWO_SDA | IO:GPIO[46] | IO:TWO_SDA | — | — | — | O:PHY_DBG[11] |
| W47 | STS0_CLK | IO:GPIO[43] | I:STS0_CLK | O:CPUPLL_CLKO | — | I:URT3_RXD | O:PHY_DBG[0] |
| R51 | STS0_SOP | IO:GPIO[42] | I:STS0_SOP | O:SYSPLL_CLKO | I:STS5_CLK | O:URT3_TXD | O:PHY_DBG[1] |
| W49 | STS0_SD | IO:GPIO[41] | I:STS0_SD | O:MEMPLL_CLKO | — | I:URT3_CTSn | O:PHY_DBG[2] |
| R53 | STS0_VALD | IO:GPIO[40] | I:STS0_VALD | — | I:STS5_SD | O:URT3_RTSn | O:PHY_DBG[3] |
| R57 | STS1_CLK | IO:GPIO[39] | I:STS1_CLK | O:PWM[0] | — | — | O:PHY_DBG[4] |
| R55 | STS1_SOP | IO:GPIO[38] | I:STS1_SOP | O:PWM[1] | I:STS6_CLK | — | O:PHY_DBG[5] |
| P59 | STS1_SD | IO:GPIO[37] | I:STS1_SD | O:PWM[2] | — | — | O:PHY_DBG[6] |
| P60 | STS1_VALD | IO:GPIO[36] | I:STS1_VALD | O:PWM[3] | I:STS6_SD | — | O:PHY_DBG[7] |
| W53 | USB2_DRV_VBUS | O:USB2_DRV_VBUS | IO:GPIO[55] | — | — | — | — |

1. Mode 0 is the default mode after reset.

Table 59. RGMII Group Multiplexing

| Ball # | Primary Pin Name | Mode 0 ¹ | Mode 1 | Mode 7 | Mode Strap |
|--------|------------------|---------------------|---------------------------|---------------|-------------------|
| T60 | RGMII_MDC | O:RGMII_MDC | IO:GPIO[29] | O:PHY_DBG[8] | — |
| W55 | RGMII_MDIO | IO:RGMII_MDIO | IO:GPIO[28] | O:PHY_DBG[9] | — |
| T61 | RGMII_TXC | O:RGMII_TXC | IO:GPIO[23] (output only) | — | legacy_boot |
| V59 | RGMII_TXD[0] | O:RGMII_TXD[0] | IO:GPIO[27] (output only) | — | software_strap[2] |
| AG47 | RGMII_TXD[1] | O:RGMII_TXD[1] | IO:GPIO[26] (output only) | O:PHY_DBG[15] | software_strap[3] |
| W59 | RGMII_TXD[2] | O:RGMII_TXD[2] | IO:GPIO[25] (output only) | — | cpuRstByps |
| Y59 | RGMII_TXD[3] | O:RGMII_TXD[3] | IO:GPIO[24] (output only) | — | pllPwrDown |
| AC51 | RGMII_TXCTL | O:RGMII_TXCTL | IO:GPIO[22] (output only) | — | pllByps |
| AG49 | RGMII_RXC | I:RGMII_RXC | IO:GPIO[31] | — | — |
| AC53 | RGMII_RXD[0] | I:RGMII_RXD[0] | IO:GPIO[35] | — | — |
| AB61 | RGMII_RXD[1] | I:RGMII_RXD[1] | IO:GPIO[34] | — | — |
| Y60 | RGMII_RXD[2] | I:RGMII_RXD[2] | IO:GPIO[33] | — | — |
| AG51 | RGMII_RXD[3] | I:RGMII_RXD[3] | IO:GPIO[32] | — | — |
| AC55 | RGMII_RXCTL | I:RGMII_RXCTL | IO:GPIO[30] | — | — |

1. Mode 0 is the default mode after reset. Strap mode is only used during power-up reset.

Table 60. AVIO_I2S Group Multiplexing

| Ball # | Primary Pin Name | Mode 0 ¹ | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 7 | Mode Strap |
|--------|------------------|---------------------|--------------|---------------|----------------|--------------|---------------|-------------|
| BD59 | I2S1_DO[0] | IO:GPIO[19] | O:I2S1_DO[0] | — | — | — | O:AVIO_DBG[4] | — |
| BF60 | I2S1_DO[1] | IO:GPIO[17] | O:I2S1_DO[1] | — | I:STS2_CLK | — | O:AVIO_DBG[5] | — |
| BH61 | I2S1_DO[2] | IO:GPIO[16] | O:I2S1_DO[2] | O:PWM[2] | I:STS2_SD | I:PDMB_DI[2] | O:AVIO_DBG[6] | — |
| BF59 | I2S1_DO[3] | IO:GPIO[15] | O:I2S1_DO[3] | O:PWM[3] | I:STS2_VALD | I:PDMB_DI[3] | O:AVIO_DBG[7] | — |
| BG55 | I2S1_LRCK | IO:GPIO[21] | IO:I2S1_LRCK | O:PWM[0] | O:ARC_TEST_OUT | — | O:AVIO_DBG[0] | — |
| BH60 | I2S1_BCLK | IO:GPIO[20] | IO:I2S1_BCLK | O:PWM[1] | — | — | O:AVIO_DBG[1] | — |
| BK59 | SPDIFO | IO:GPIO[14] | O:SPDIFO | — | — | O:AVPLL_CLKO | — | boot_src[1] |
| BL59 | SPDIFI | IO:GPIO[4] | I:SPDIFI | I:PDMC_DI | — | — | — | — |
| BM60 | I2S2_LRCK | IO:GPIO[13] | IO:I2S2_LRCK | — | — | — | — | — |
| BP60 | I2S2_BCLK | IO:GPIO[12] | IO:I2S2_BCLK | IO:PDMA_CLKIO | — | — | — | — |
| BT59 | I2S2_DI[0] | IO:GPIO[11] | I:I2S2_DI[0] | I:PDMA_DI[3] | — | — | — | — |
| BM59 | I2S2_DI[1] | IO:GPIO[10] | I:I2S2_DI[1] | I:PDMA_DI[2] | I:STS4_VALD | — | — | — |
| BT61 | I2S2_DI[2] | IO:GPIO[9] | I:I2S2_DI[2] | I:PDMA_DI[1] | I:STS4_CLK | — | — | — |
| BT60 | I2S2_DI[3] | IO:GPIO[8] | I:I2S2_DI[3] | I:PDMA_DI[0] | I:STS4_SD | — | — | — |
| BG53 | I2S1_MCLK | IO:GPIO[18] | IO:I2S1_MCLK | — | I:STS2_SOP | — | O:AVIO_DBG[3] | — |
| BP61 | I2S2_MCLK | IO:GPIO[7] | IO:I2S2_MCLK | IO:PDMB_CLKIO | — | O:HDMI_FBCLK | — | boot_src[0] |
| BL49 | HDMI_TX_EDDC_SCL | IO:HDMI_TX_EDDC_SCL | IO:GPIO[6] | — | — | — | — | — |
| BL51 | HDMI_TX_EDDC_SDA | IO:HDMI_TX_EDDC_SDA | IO:GPIO[5] | — | — | — | — | — |
| BY59 | I2S3_DO | IO:GPIO[1] | O:I2S3_DO | — | I:STS3_SOP | — | O:AVIO_DBG[2] | — |
| BV59 | I2S3_LRCK | IO:GPIO[3] | IO:I2S3_LRCK | — | I:STS3_CLK | — | — | — |
| CA58 | I2S3_BCLK | IO:GPIO[2] | IO:I2S3_BCLK | — | I:STS3_SD | — | — | — |
| CA59 | I2S3_DI | IO:GPIO[0] | I:I2S3_DI | — | I:STS3_VALD | — | — | — |

1. Mode 0 is the default mode after reset. Strap mode is only used during power-up reset.

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Stresses above those listed in the Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 61. Absolute Maximum Ratings

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|---|------|-----|---|-------|
| VDDIO1P8 | All IO supply voltage at 1.8V | -0.3 | — | 1.98 | V |
| AVDD1P8 | All Analog supply voltage at 1.8V | -0.3 | — | 1.98 | |
| SDIO_VDDIO3P3 | SDIO IO supply voltage at 3.3V | -0.3 | — | 3.63 | |
| AVDD3P3 | All analog supply voltage at 3.3V | -0.3 | — | 3.63 | |
| AVDD | All analog supply voltage at 0.8V | -0.1 | — | 1.12 | |
| DVDD | All digital supply voltage at 0.8V | -0.1 | — | 1.12 | |
| SM_VDD_CORE | SM Core supply voltage | -0.1 | — | 0.96 | |
| VDD_CPU | CPU supply Voltage | -0.1 | — | 1.12 | |
| VDD_CORE | CORE supply voltage | -0.1 | — | 1.12 | |
| M0_AVDD1P8 | MEMPLL analog power at 1.8V | -0.3 | — | 1.98 | |
| VDDQ | LPDDR4 IO power at 1.1V | -0.3 | — | 1.21 | |
| VDDQLP | LPDDR4(x) IO power at 1.1V or 0.6V | -0.3 | — | 1.21 | |
| V _{IN} | Input signals supplied by SDIO_VDDIO3P3 | -0.3 | — | 3.63 | |
| V _{OUT} | Output signals supplied by SDIO_VDDIO3P3 | -0.3 | — | 3.63 | |
| V _{PIN} | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TWO_SCL, TWO_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMIRX_HPD, SM_HDMIRX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | -0.3 | — | 1.98 | |
| | Other input and output signals supplied by VDDIO1P8 | | | 1.98 or VDDIO1P8 +0.2 whichever is less | |
| T _{STORAGE} | Storage temperature | -55 | — | +125 ¹ | °C |

1. 125 °C is the re-bake temperature. For extended storage time greater than 24 hours, +85 °C should be the maximum.

3.2. Recommended Operating Conditions

Table 62. Recommended Operating Conditions

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------------------|---|------------|-------|-----------|-------|-------|
| VDDIO1P8 | All IO supply voltage at 1.8V | — | 1.71 | 1.8 | 1.89 | V |
| AVDD1P8 | All analog supply voltage at 1.8V | — | 1.71 | 1.8 | 1.89 | |
| SDIO_VDDIO3P3 | SDIO IO supply voltage at 3.3V | — | 3.135 | 3.3 | 3.465 | |
| AVDD3P3 | All analog supply voltage at 3.3V | — | 3.135 | 3.3 | 3.465 | |
| AVDD | All analog supply voltage at 0.8V | Consumer | 0.72 | — | 0.958 | |
| | | Industrial | 0.72 | — | 0.998 | |
| DVDD | All digital supply voltage at 0.8V | Consumer | 0.72 | — | 0.958 | |
| | | Industrial | 0.72 | — | 0.998 | |
| SM_VDD_CORE | SM Core supply voltage | — | 0.72 | — | 0.88 | |
| VDD_CPU ¹ | CPU supply voltage | Consumer | 0.72 | 0.8 | 1.037 | |
| | | Industrial | 0.72 | 0.8 | 1.076 | |
| VDD_CORE ¹ | CORE supply voltage | Consumer | 0.72 | 0.8 | 0.958 | |
| | | Industrial | 0.72 | 0.8 | 0.998 | |
| VDD_CPU-VDD_CORE | Difference between CPU and CORE supplies ² | — | -100 | — | 100 | mV |
| M0_AVDD1P8 | MEMPLL analog power at 1.8V | — | 1.71 | 1.8 | 1.89 | V |
| VDDQ | LPDDR4 IO power at 1.1V | — | 1.06 | 1.1 | 1.17 | |
| VDDQLP | LPDDR4 IO power at 1.1V | — | 1.06 | 1.1 | 1.17 | |
| | LPDDR4x IO power at 0.6V | — | 0.57 | 0.6 | 0.63 | |
| T _A | Ambient operating temperature ³ | Consumer | 0 | — | 70 | °C |
| | | Industrial | -40 | — | 85 | |
| T _J | Junction temperature | Consumer | 0 | — | 105 | |
| | | Industrial | -40 | — | 125 | |
| R _{MO_CAL} | LPDDR4 reference current resistor, connect to VSS | — | — | 120± 1% | — | ohm |
| R _{USB2_REXT} | USB 2.0 PHY reference current resistor, connect to AVSS | — | — | 200± 1% | — | |
| R _{USB2_VBUS_REXT} | USB 2.0 PHY VBUS pin isolation resistor, connect to 5V VBUS voltage on USB link | — | — | 30K± 1% | — | |
| R _{USB3_REXT} | USB 3.0 PHY reference current resistor, connect to AVSS | — | — | 200± 1% | — | |
| R _{USB3_VBUS_REXT} | USB 3.0 PHY VBUS pin isolation resistor, connect to 5V VBUS voltage on USB link | — | — | 30K± 1% | — | |
| R _{PCIE_REXT} | PCIE PHY reference current resistor, connect to AVSS | — | — | 200± 1% | — | |
| R _{HDMI_TX_REXT} | HDMI TX reference current resistor, connect to AVSS | — | — | 1.62K± 1% | — | |
| R _{HDMI_RX_REXT} | HDMI RX reference current resistor, connect to AVSS | — | — | 200± 1% | — | |
| R _{MIPI_DSI_REXT} | MIPI DSI reference current resistor, connect to AVSS | — | — | 200± 1% | — | |
| R _{MIPI_CSI_REXT} | MIPI CSI reference current resistor, connect to AVSS | — | — | 200± 1% | — | |

- The optimum core supply voltage is determined by the individual chip manufacturing process variation. The system software reads an index stored in the on-chip OTP memory and controls the VDD regulator output voltage. The nominal regulation of the VDD regulator should be within ±3%. For details refer to the *PV Compensation Application Note*.
- For normal operation only, not applicable during power up/down.
- The important parameter is maximum junction temperature. The maximum junction temperature needs to be observed in addition to the ambient temperature limits.

3.2.1. Power-up Sequence

This section discusses the recommended power-up sequence.

Table 63. SL1680 Power-up Requirement

| Power-up Timing Parameter | Power Rails | Min | Typ | Max | Units |
|---|--------------------------------------|-----|-----|-----|-------|
| Ramp rate | VDD_CORE, VDD_CPU | — | — | 32 | mV/uS |
| | All of DVDD | — | — | 32 | |
| | All of AVDD | | | | |
| | All of VDDIO1P8 | — | — | 18 | |
| | All of AVDD1P8 | | | | |
| | VDDQLP | — | — | 5 | |
| | VDDQ | | | 100 | |
| | All of AVDD3P3 | | | | |
| | SDIO_VDDIO3P3 | — | — | 5.1 | |
| MO_AVDD1P8 | | | | | |
| T1-T0, Time duration between power rails ramp | VDD_CORE and SoC AVDD1P8 power rails | 0 | — | — | mS |

Table 64. On-chip Power-on-Reset (PoR) Thresholds

| Parameter | Description | Min | Typ | Max | Units |
|-----------|----------------|------|------|------|-------|
| CORE POR | V_{thl} | 0.44 | 0.49 | 0.53 | V |
| | V_{tlh} | 0.48 | 0.51 | 0.57 | |
| IO POR | V_{tlh_1P8} | 1.32 | 1.38 | 1.49 | |
| | V_{thl_1P8} | 1.32 | 1.38 | 1.49 | |
| | V_{tlh_3P3} | 2.35 | 2.5 | 2.67 | |
| | V_{thl_3P3} | 2.35 | 2.5 | 2.67 | |

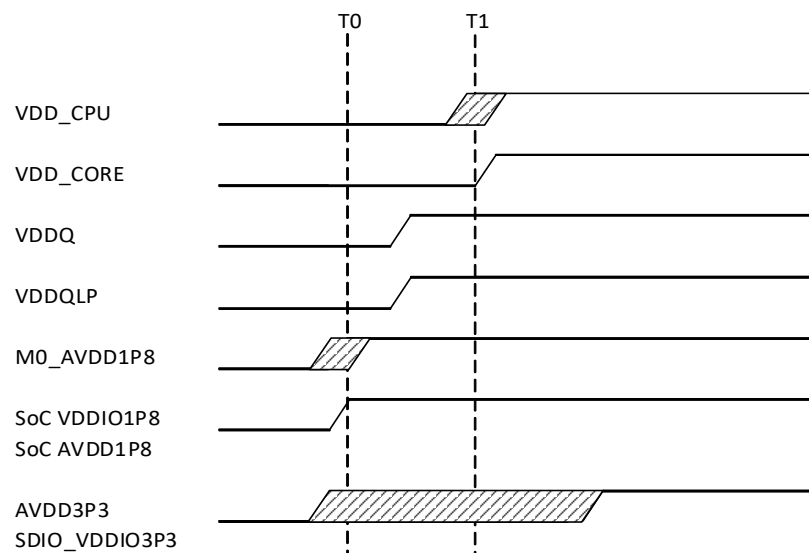


Figure 4. SL1680 Recommended power-up sequence in SoC power domain

Note:

1. VDD_CORE starts ramping up (T1) after SoC AVDD1P8 reaches its 100% of 1.8V (T0).
2. MO_AVDD1P8, VDDQ and VDDQLP shall follow the power sequence requirement from the DRAM devices if shared with the DRAM. Otherwise, no specific sequence required between them or relative to other power rails.
3. VDD_CPU and VDD_CORE are recommended to ramp up relatively close to each other. No specific sequence is required between them.
4. No specific sequence is required regarding the SoC 3.3V power rails.
5. No specific sequence is required between SM power rails, or between SM and SoC power rails.
6. Follow the above power sequence requirements when returning from a partially powered-off state such as low-power standby.

3.3. Crystal Specifications

Table 65. Crystal Specifications

| Parameter | Condition | Typical | Unit |
|-----------------------|--|---------------|------|
| Fundamental Frequency | — | 25 | MHz |
| Frequency Tolerance | 0 - 70 °C (for consumer) -40 - 85 °C (for industrial) | $\leq \pm 50$ | ppm |
| Load Capacitance | — | g^1 | pF |
| Max. ESR | — | 60 | ohm |
| Drive Level | — | 35 | uW |
| Mode of Oscillation | — | Fundamental | — |

1. For more design details, please contact the Synaptics application engineering team.

3.4. Thermal Conditions for the SL1680 Device 605-pin BGA Package

Table 66. Thermal Conditions¹ for the SL1680 Device

| Symbol | Parameter | Condition | Spec. | Min | Typ | Max | Units |
|---|--|---|------------|-----|---------|-----|-------|
| θ_{JA} | Thermal resistance-junction to ambient of the SL1680 device 605-pin BGA package $\theta_{JA} = (T_J - T_A) / P$ P = Total Power Dissipation | JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow | Consumer | — | 12.41 | — | |
| | | | Industrial | — | 10.96 | — | |
| | | JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | Consumer | — | 10.79 | — | |
| | | | Industrial | — | — | — | |
| | | JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | Consumer | — | 10.15 | — | |
| | | | Industrial | — | 10.448 | — | |
| JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | Consumer | — | — | — | | | |
| | Industrial | — | 9.676 | — | | | |
| ψ_{JT} | Thermal characteristic parameter-junction to top center of the SL1680 device 605-pin BGA package $\psi_{JT} = (T_J - T_{TOP}) / P$ T_{TOP} = Temperature on the top center of the package | JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow | Consumer | — | 0.04 | — | °C/W |
| | | | Industrial | — | 0.01655 | — | |
| | | JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | Consumer | — | 0.03 | — | |
| | | | Industrial | — | — | — | |
| | | JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | Consumer | — | 0.03 | — | |
| | | | Industrial | — | 0.0176 | — | |
| JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | Consumer | — | — | — | | | |
| | Industrial | — | 0.0178 | — | | | |
| θ_{JC} | Thermal resistance-junction to case of the SL1680 device 605-pin BGA package $\theta_{JC} = (T_J - T_C) / P_{TOP}$ P_{TOP} = Power Dissipation from the top of the package | JEDEC with no air flow | Consumer | — | 0.10 | — | |
| | | | Industrial | — | 0.082 | — | |
| θ_{JB} | Thermal resistance-junction to board of the SL1680 device 605-pin BGA package $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface. | JEDEC with no air flow | Consumer | — | 4.32 | — | |
| | | | Industrial | — | 3.153 | — | |

1. For definitions and usage of the thermal parameters in this table, refer to JESD51-12.01.

3.5. AC and DC Electrical Characteristics

3.5.1. Digital Pins Operating Conditions

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless otherwise specified.)

Table 67. Digital Operating Conditions (Sheet 1 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-----------------|--|--------------------------|-----------|---------------|-----|---------------|-------|
| V _{IH} | High level input voltage with Schmitt Trigger disabled | All 1.8V Digital IO pins | — | 0.65*VDDIO1P8 | — | 1.98 | V |
| | | HDMI_TX_HPD | — | 2.0 | — | 5.3 | |
| V _{IL} | Low level input voltage with Schmitt Trigger disabled | All 1.8V Digital IO pins | — | -0.3 | — | 0.35*VDDIO1P8 | |
| | | HDMI_TX_HPD | — | 0 | — | 0.8 | |

Table 67. Digital Operating Conditions (Sheet 2 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|----------|--|--|------------------------|------|------|------|-------|
| V_{T+} | Low to High Threshold Point with Schmitt Trigger enabled | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMIRX_HPD, SM_HDMIRX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 0.98 | 1.09 | 1.21 | V |
| | | SDIO_DATA[3:0] SDIO_CMD | SDIO VIO under 1.8V | 1.07 | — | — | |
| | | | SDIO VIO under 3.3V | 1.68 | — | — | |
| | | EMMC_DATA[7:0] EMMC_CMD EMMC_STRB | — | 1.07 | — | — | |
| | | SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn | — | 0.95 | 1.06 | 1.16 | |
| | Other 1.8V digital IO pins | — | 1 | 1.12 | 1.23 | | |

Table 67. Digital Operating Conditions (Sheet 3 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|----------------|--|--|------------------------|------|------|------|-------|
| V _T | High to Low Threshold Point with Schmitt Trigger enabled | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMI_RX_HPD, SM_HDMI_RX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 0.76 | 0.86 | 0.97 | V |
| | | SDIO_DATA[3:0] SDIO_CMD | SDIO VIO under 1.8V | — | — | 0.68 | |
| | | | SDIO VIO under 3.3V | — | — | 0.9 | |
| | | EMMC_DATA[7:0] EMMC_CMD EMMC_STRB | — | — | — | 0.68 | |
| | | SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn | — | 0.68 | 0.76 | 0.85 | |
| | Other 1.8V digital IO pins | — | 0.67 | 0.76 | 0.84 | | |

Table 67. Digital Operating Conditions (Sheet 4 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-----------------|--------------------|--|-----------|-----|-----|------|-------|
| R _{PU} | Pull-up Resistor | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMI_RX_HPD, SM_HDMI_RX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 32K | 48K | 79K | Ohm |
| | | SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn | — | 57K | 87K | 146K | |
| | | Other 1.8V digital IO pins ¹ | — | 19K | 26K | 39K | |
| R _{PD} | Pull-down Resistor | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMI_RX_HPD, SM_HDMI_RX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 30K | 44K | 68K | Ohm |
| | | SM_POR_EN SM_RSTIn SM_TEST_EN SM_JTAG_SEL SM_TCK SM_TRSTn | — | 54K | 79K | 127K | |
| | | Other 1.8V digital IO pins ¹ | — | 18K | 24K | 34K | |

Table 67. Digital Operating Conditions (Sheet 5 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|------------------|--------------|--|-----------|------|------|------|-------|
| I_{OL} @ 0.45V | DS[3:0]=0000 | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMI_RX_HPD, SM_HDMI_RX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 0.7 | 1.1 | 1.4 | mA |
| | DS[3:0]=0001 | | | 1.1 | 1.6 | 2.1 | |
| | DS[3:0]=0010 | | | 2.2 | 3.2 | 4.1 | |
| | DS[3:0]=0011 | | | 3.3 | 4.8 | 6.2 | |
| | DS[3:0]=0100 | | | 4.4 | 6.4 | 8.2 | |
| | DS[3:0]=0101 | | | 5.5 | 7.9 | 10.2 | |
| | DS[3:0]=0110 | | | 6.6 | 9.5 | 12.3 | |
| | DS[3:0]=0111 | | | 7.7 | 11.1 | 14.3 | |
| | DS[3:0]=1000 | | | 8.8 | 12.6 | 16.2 | |
| | DS[3:0]=1001 | | | 9.8 | 14.2 | 18.3 | |
| | DS[3:0]=1010 | | | 10.9 | 15.8 | 20.3 | |
| | DS[3:0]=1011 | | | 12 | 17.4 | 22.3 | |
| | DS[3:0]=1100 | | | 13.1 | 18.8 | 24.1 | |
| | DS[3:0]=1101 | | | 14.2 | 20.4 | 26.1 | |
| | DS[3:0]=1110 | | | 15.2 | 22 | 28.1 | |
| | DS[3:0]=1111 | 16.3 | 23.5 | 30.1 | | | |
| | DS[2:0]=000 | Other 1.8V digital IO pins ¹ | — | 2.2 | 3.1 | 4.1 | |
| | DS[2:0]=001 | | | 4.6 | 6.7 | 8.7 | |
| | DS[2:0]=010 | | | 6.6 | 9.6 | 12.5 | |
| | DS[2:0]=011 | | | 8.9 | 12.8 | 16.7 | |
| DS[2:0]=100 | 12.3 | | | 17.8 | 23.1 | | |
| DS[2:0]=101 | 14.3 | | | 20.7 | 26.8 | | |
| DS[2:0]=110 | 15.8 | | | 22.9 | 29.6 | | |
| DS[2:0]=111 | 17.6 | | | 25.5 | 33 | | |

Table 67. Digital Operating Conditions (Sheet 6 of 6)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|------------------------------|---|--|---------------------|------|------|------|-------|
| I_{OH} @ VDDIO-0.45 | DS[3:0]=0000 | SDIO_CDn, SDIO_WP, SPI1_SS2n, SPI1_SS3n, TW0_SCL, TW0_SDA, SM_TW2_SCL, SM_TW2_SDA, SM_URT1_TXD, SM_URT1_RXD, SM_HDMI_HPD, SM_HDMI_CEC, SM_TW3_SCL, SM_TW3_SDA, SM_URTO_TXD, SM_URTO_RXD, SM_HDMI_RX_HPD, SM_HDMI_RX_PWR5V, HDMI_TX_EDDC_SCL, HDMI_TX_EDDC_SDA | — | 0.7 | 1.1 | 1.5 | mA |
| | DS[3:0]=0001 | | | 1.1 | 1.7 | 2.3 | |
| | DS[3:0]=0010 | | | 2.2 | 3.3 | 4.5 | |
| | DS[3:0]=0011 | | | 3.2 | 5.0 | 6.7 | |
| | DS[3:0]=0100 | | | 4.3 | 6.6 | 8.9 | |
| | DS[3:0]=0101 | | | 5.4 | 8.2 | 11.1 | |
| | DS[3:0]=0110 | | | 6.4 | 9.8 | 13.2 | |
| | DS[3:0]=0111 | | | 7.5 | 11.5 | 15.4 | |
| | DS[3:0]=1000 | | | 8.5 | 13.0 | 17.4 | |
| | DS[3:0]=1001 | | | 9.6 | 14.7 | 19.6 | |
| | DS[3:0]=1010 | | | 10.6 | 16.3 | 21.8 | |
| | DS[3:0]=1011 | | | 11.7 | 17.9 | 23.9 | |
| | DS[3:0]=1100 | | | 12.7 | 19.4 | 25.9 | |
| | DS[3:0]=1101 | | | 13.8 | 21.0 | 28.0 | |
| | DS[3:0]=1110 | | | 14.8 | 22.6 | 30.0 | |
| DS[3:0]=1111 | 15.8 | 24.2 | 32.2 | | | | |
| I_{OH} @VDDIO- 0.45V | DS[2:0]=000 | Other 1.8V digital IO pins ¹ | — | 1.8 | 2.8 | 3.7 | mA |
| | DS[2:0]=001 | | | 3.9 | 5.9 | 7.8 | |
| | DS[2:0]=010 | | | 5.6 | 8.4 | 11.2 | |
| | DS[2:0]=011 | | | 7.5 | 11.2 | 15.0 | |
| | DS[2:0]=100 | | | 10.4 | 15.5 | 20.6 | |
| | DS[2:0]=101 | | | 12.0 | 18.1 | 23.9 | |
| | DS[2:0]=110 | | | 13.3 | 20.0 | 26.5 | |
| | DS[2:0]=111 | | | 14.8 | 22.2 | 29.5 | |
| Input Capacitance | — | — | — | — | — | 3.2 | pF |
| I_I | Input Leakage Current | — | $V_I=1.8V$ or 0V | — | — | ±10 | μA |
| I_{OZ} | Tri-state Output Leakage Current | — | $V_O=1.8V$ or 0V | — | — | ±10 | |

1. eMMC and SDIO pins are not included unless specified.

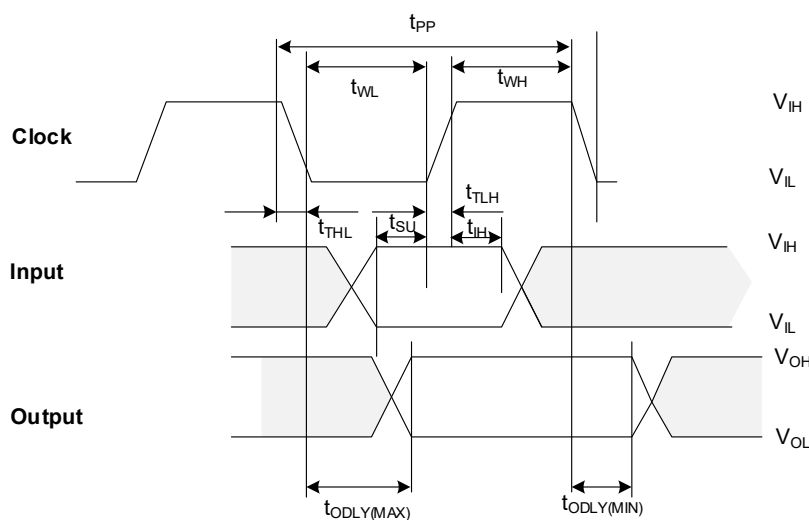
3.5.2. SD, SDIO Timing

3.5.2.1. SD, SDIO Default Mode Timing Parameters

(Over full range of values listed in Table 62, Recommended Operating Conditions unless otherwise specified.)

Table 68. SD, SDIO Default Mode Timing Parameters

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|-------------------------------------|---------------------|-----|-----|-----|-------|
| f_{PP} | Clock Frequency Data Transfer Mode | — | 0 | 25 | 25 | MHz |
| f_{OD} | Clock Frequency Identification Mode | — | 0 | — | 400 | kHz |
| t_{WL} | Clock Low time | — | 10 | — | — | ns |
| t_{WH} | Clock High time | — | 10 | — | — | |
| t_{TLH} | Clock Rise time | — | — | — | 10 | |
| t_{THL} | Clock Fall time | — | — | — | 10 | |
| Inputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{iSU} | Input Setup time | — | — | — | — | ns |
| t_{iH} | Input Hold time | — | — | — | — | |
| Outputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ODLY} | Output delay time | Data Transfer Mode | 0 | — | 14 | ns |
| t_{ODLY} | Output delay time | Identification Mode | 0 | — | 50 | |



Shaded areas are not valid

Figure 5. Timing Diagram Data Input/Output Referenced to Clock (Default)

3.5.2.2. SD, SDIO High-speed Mode Timing Parameters

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless otherwise specified.)

Table 69. SD, SDIO High-Speed Mode Timing Parameters

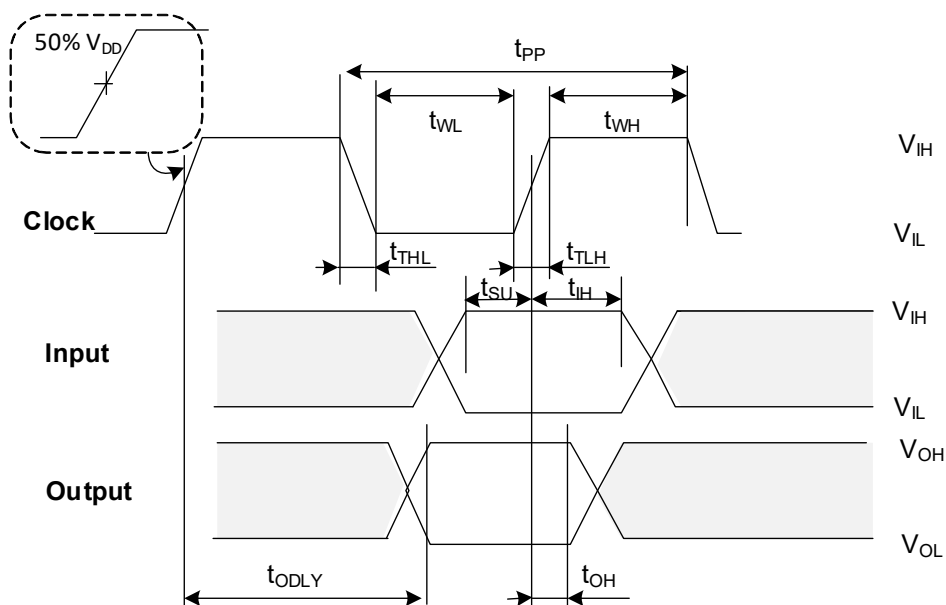
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|------------------------------------|--------------------|-----|-----|-----|-------|
| f_{PP} | Clock Frequency Data Transfer Mode | – | 0 | 50 | 50 | MHz |
| t_{WL} | Clock Low time | – | 7 | – | – | ns |
| t_{WH} | Clock High time | – | 7 | – | – | |
| t_{TLH} | Clock Rise time | – | – | – | 3 | |
| t_{THL} | Clock Fall time | – | – | – | 3 | |
| Inputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ISU} | Input Setup time | – | – | – | – | ns |
| t_{IH} | Input Hold time | – | – | – | – | |
| Outputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ODLY} | Output Delay time | Data Transfer mode | 0 | – | 14 | ns |
| t_{OH} | Output Hold time | – | 2.5 | – | – | |

3.5.2.3. SD, SDIO SDR104 Mode Timing Parameters

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless otherwise specified.)

Table 70. SD, SDIO SDR104 Mode Timing Parameters

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|------------------------------------|-----------|------|-----|------|-------|
| f_{PP} | Clock Frequency Data Transfer Mode | – | 0 | 208 | 208 | MHz |
| t_{WL} | Clock Low time | – | 1.44 | – | – | ns |
| t_{WH} | Clock High time | – | 1.44 | – | – | |
| t_{TLH} | Clock Rise time | – | – | – | 0.96 | |
| t_{THL} | Clock Fall time | – | – | – | 0.96 | |
| Inputs DAT (referenced to Clock): | | | | | | |
| t_{ISU} | Input Setup time | – | – | – | – | ns |
| t_{IH} | Input Hold time | – | – | – | – | |



Shaded areas are not valid

Figure 6. Timing Diagram Data Input/Output Referenced to Clock (High-speed and SDR104 mode)

3.5.3. Two-Wire Serial Interface (TWSI) Timing

3.5.3.1. TWSI Standard and Fast Mode Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless otherwise specified.)

Table 71. TWSI Standard and Fast Mode Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------------|---|-----------|------|-----|------|-------|
| F _{TWSI_SCL} | SCL Clock Frequency | 100 kHz | – | – | 100 | kHz |
| | | 400 kHz | – | – | 400 | |
| T _{TWSI_NS} | Noise Suppression Time at SCL, SDA Inputs | 100 kHz | – | – | 80 | ns |
| | | 400 kHz | – | – | 80 | |
| T _{TWSI_R} | SCL, SDA Rise time | 100 kHz | – | – | 1000 | |
| | | 400 kHz | – | – | 300 | |
| T _{TWSI_F} | SCL, SDA Fall Time | 100 kHz | – | – | 300 | |
| | | 400 kHz | – | – | 300 | |
| T _{TWSI_HIGH} | Clock High Period | 100 kHz | 4000 | – | – | |
| | | 400 kHz | 600 | – | – | |
| T _{TWSI_LOW} | Clock Low Period | 100 kHz | 4700 | – | – | |
| | | 400 kHz | 1300 | – | – | |
| T _{TWSI_SU:STA} | Start Condition Setup Time (for a Repeated Start Condition) | 100 kHz | 4700 | – | – | |
| | | 400 kHz | 600 | – | – | |
| T _{TWSI_HD:STA} | Start Condition Hold Time | 100 kHz | 4000 | – | – | |
| | | 400 kHz | 600 | – | – | |
| T _{TWSI_SU:STO} | Stop Condition Setup Time | 100 kHz | 4000 | – | – | |
| | | 400 kHz | 600 | – | – | |
| T _{TWSI_SU:DAT} | Data in Setup Time | 100 kHz | 250 | – | – | |
| | | 400 kHz | 100 | – | – | |
| T _{TWSI_HD:DAT} | Data in Hold Time | 100 kHz | 0 | – | – | |
| | | 400 kHz | 0 | – | – | |
| T _{TWSI_BUF} | Bus Free Time | 100 kHz | 4700 | – | – | |
| | | 400 kHz | 1300 | – | – | |
| T _{TWSI_DLY} | SCL Low to SDA Data Out Valid | 100 kHz | 40 | – | 200 | |
| | | 400 kHz | 40 | – | 200 | |

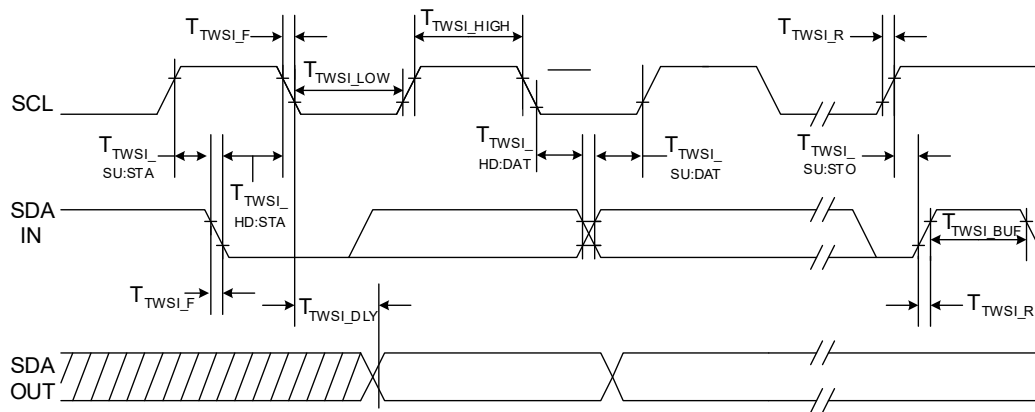


Figure 7. Two-Wire Serial Interface Timing

3.5.4. RGMII Timing

Table 72. RGMII Interface Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------------|--|------|-----|------|-------|
| T_{skewT} | Data to Clock output Skew (at transmitter) | -500 | 0 | 500 | ps |
| T_{skewR} | Clock to Data input Skew (at receiver) | 1.0 | — | 2.6 | ns |
| T_{CYCLE} | Clock Cycle Duration | 7.2 | 8.0 | 8.8 | |
| $T_{CYCLE_HIGH1000}$ | High Time for 1000BASE-T ¹ | 3.6 | 4.0 | 4.4 | |
| T_{RISE}/T_{FALL} | Rise/Fall Time (20–80%) | — | — | 0.75 | |

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{CYCLE} of the lowest speed transitioned between.

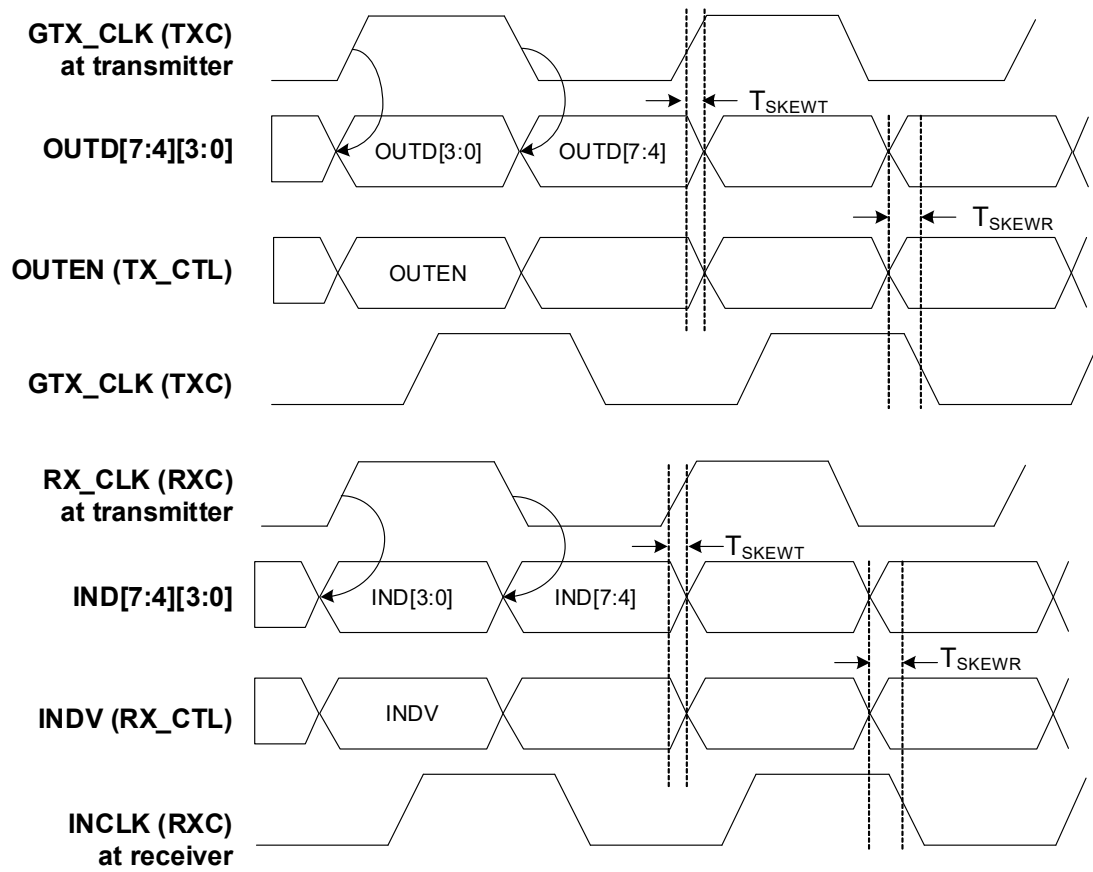


Figure 8. RGMII Multiplexing and Timing

3.5.5. SPI Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 73. SCLK Cycle Time Configurable Range

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|-------------------------|--|-----|-----|-----------|-------|
| T_{SCLK} | SoC SPI SCLK cycle time | 100 MHz SoC SPI controller input clock | 20 | — | 655,340 | ns |
| T_{SCLK} | SM SPI SCLK cycle time | 25 MHz SM SPI controller input clock | 80 | — | 2,621,360 | |

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 74. Motorola SPI Mode 0/2 Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|---|--|------|-----|------|------------|
| T_{LS1} | Time from SSn assertion to the first SCLK active edge | The first SPI cycle in a transfer | — | 1.5 | — | T_{SCLK} |
| | | Subsequent SPI cycles | — | 0.5 | — | |
| T_{LS2} | Time from the last SCLK inactive edge to SSn de-assertion | Other than the last SPI cycle | — | 0.5 | — | |
| | | The last SPI cycle in a transfer | — | 1.0 | — | |
| T_{CH} | SCLK high time | — | — | 0.5 | — | |
| T_{CL} | SCLK low time | — | — | 0.5 | — | |
| T_{LH} | SSn de-assertion Time between SPI cycles | If Tx FIFO is not empty at the end of the previous SPI cycle | — | 0.5 | — | |
| | | If Tx FIFO is empty | 2 | — | — | |
| T_{SET} | Setup time MISO with regard to SCLK active edge | — | 13.8 | — | — | ns |
| T_{HOLD} | Hold time MISO with regard to SCLK active edge | — | 0 | — | — | |
| T_{VAL1} | Time from SSn assertion to MOSI MSB valid | The first SPI cycle in a transfer | — | 1 | — | T_{SCLK} |
| | | Subsequent SPI cycles | — | 0 | — | |
| T_{VAL2} | Time from SCLK inactive edge to MOSI data valid | — | 0.12 | — | 1.28 | ns |

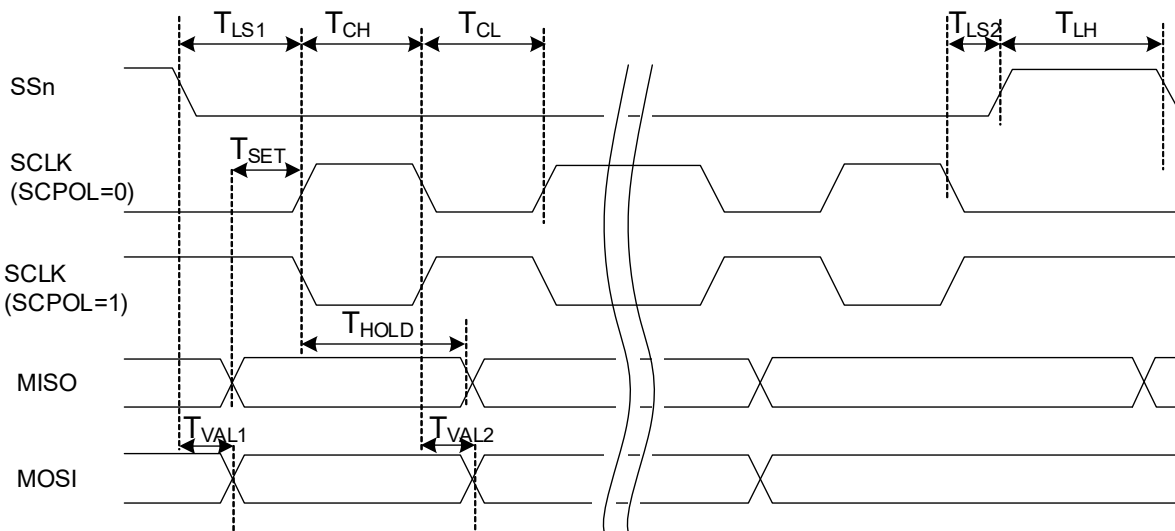


Figure 9. Motorola SPI Mode 0/2 (SCPH = 0)

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 75. Motorola SPI Mode 1/3 Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|---|--|-----|-----|-----|------------|
| T_{LS1} | Time from SSn assertion to the first SCLK active edge | — | — | 1.0 | — | T_{SCLK} |
| T_{LS2} | Time from the last SCLK inactive edge to SSn de-assertion | — | — | 1.0 | — | |
| T_{CH} | SCLK high time | — | — | 0.5 | — | |
| T_{CL} | SCLK low time | — | — | 0.5 | — | |
| T_{LH} | SSn de-assertion Time between SPI cycles | If Tx FIFO is not empty at the end of the previous SPI cycle | — | 0 | — | T_{SCLK} |
| | | If Tx FIFO is empty | 1.5 | — | — | |
| T_{SET} | Setup time MISO with regard to SCLK active edge | — | — | 30 | — | ns |
| T_{HOLD} | Hold time MISO with regard to SCLK active edge | — | — | 30 | — | |
| T_{VAL1} | Time from SSn assertion to MOSI MSB valid | The first SPI cycle in a transfer | — | 1 | — | T_{SCLK} |
| | | Subsequent SPI cycles | — | 0 | — | |
| T_{VAL2} | Time from SCLK inactive edge to MOSI data valid | — | — | 0.5 | — | ns |

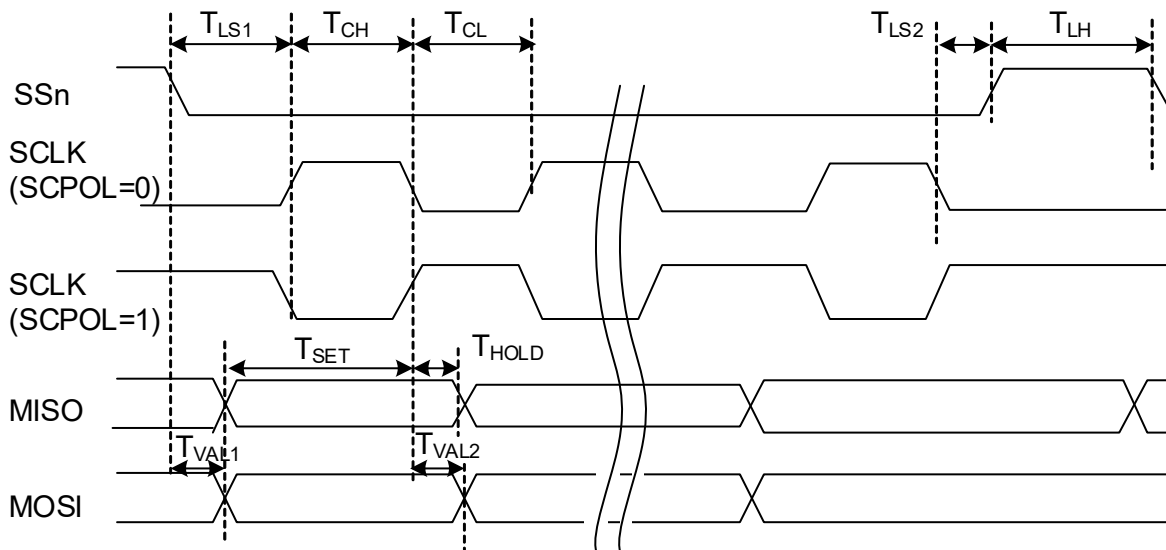


Figure 10. Motorola SPI Mode 1/3 (SCPH = 1)

3.5.6. UART Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 76. UART Timing

| Symbol | Parameter | Condition | Min | Typ ¹ | Max | Units |
|--------|--------------|-----------|-----|------------------|-----|-------|
| — | Tx bit width | ±5% | — | 8.68 | — | μs |
| — | Rx bit width | ±5% | — | 8.68 | — | |

1. The typical values are for 115.2 kbaud. Other baud rates may apply.

3.5.7. JTAG Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 77. JTAG Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|-------------------------|-----------|-----|-----|-----|-----------|
| T_{CLK} | Clock cycle | — | — | 200 | — | ns |
| $T_{ISTRSTn}$ | Set-up time for TRSTn | — | 25% | — | — | T_{clk} |
| $T_{IHTRSTn}$ | Hold time for TRSTn | — | 0 | — | — | ns |
| T_{ISTDI} | Set-up time for TDI | — | 30% | — | — | T_{clk} |
| T_{IHTDI} | Hold time for TDI | — | 0 | — | — | ns |
| T_{OHTDO} | Hold time for TDO | — | 0 | — | — | |
| T_{OVTDO} | Data valid time for TDO | — | — | — | 65% | T_{clk} |
| T_{RJT} | Rise time for all I/O | 20-80% | 10 | — | — | ns |
| T_{FJT} | Fall time for all I/Os | 80-20% | 10 | — | — | |

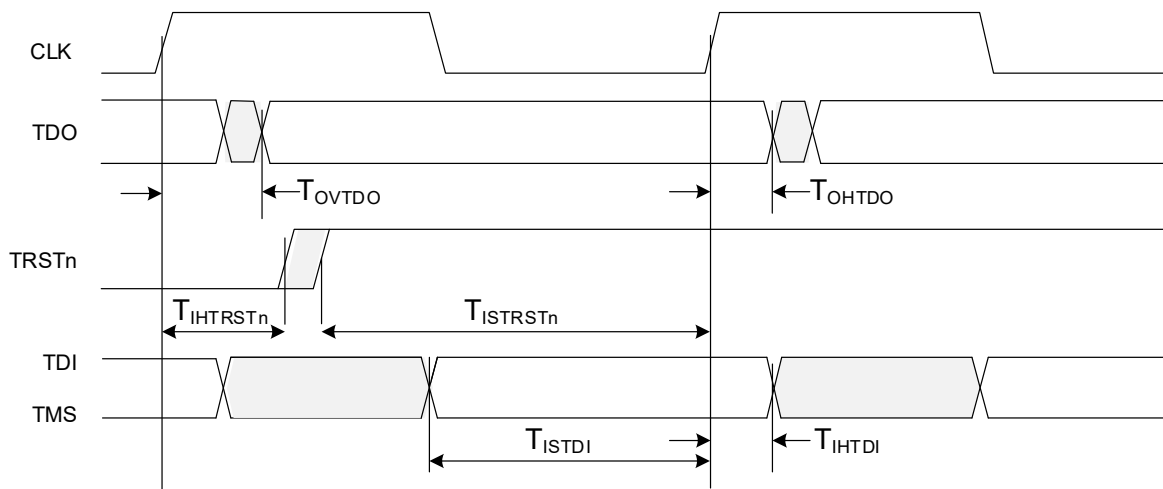


Figure 11. JTAG Timing

3.5.8. Transport Stream Serial Input Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 78. Transport Stream Serial Input Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|--|-----------|-----|-----|-----|-------|
| f_{CLK}^1 | Input Clock Frequency | — | — | 27 | 100 | MHz |
| — | Clock Duty Cycle | — | 30 | 50 | 70 | % |
| T_{IS} | Transport Stream Serial Input set-up time for STS_DATA, STS_VALID, and STS_SOP | — | 1 | — | — | ns |
| T_{IH} | Transport Stream Serial Input hold time for STS_DATA, STS_VALID, and STS_SOP | — | 1 | — | — | |

1. $f_{clk} = 1/t_{clk}$

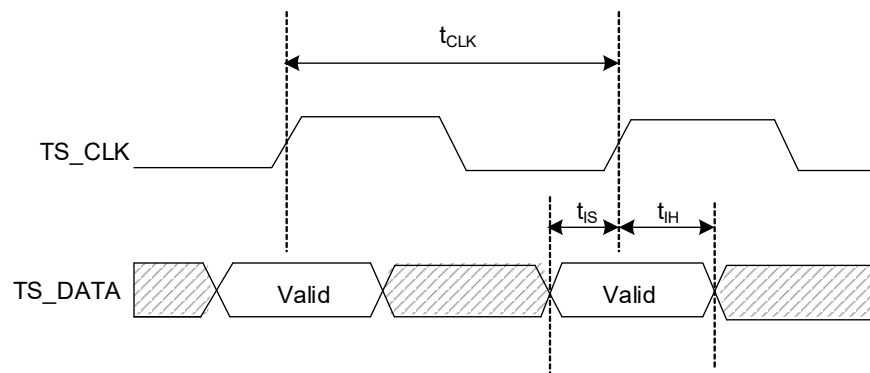


Figure 12. Transport Stream Serial Input Timing

3.5.9. I2S Timing

3.5.9.1. I2S Master Mode Timing

(Over full range of values listed in Table 62, Recommended Operating Conditions unless specified.)

Table 79. I2S Master Mode Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|---|-----------|-------|----------------------------|--------|-------|
| F_{BCLK} | BCLK Frequency | — | 16Fs | — | 64Fs | Hz |
| F_{BCLK_PCM} | BCLK Frequency in PCM Mono mode | — | 8Fs | — | 256Fs | |
| F_{BCLK_TDM} | BCLK Frequency in TDM mode | — | 16Fs | — | 256Fs | |
| F_S | — | — | 32 | — | 192 | kHz |
| D_{BCLK} | BCLK duty cycle | — | — | 50 | — | % |
| T_{SDPD}^1 | BCLK rising edge to SDATA output valid | — | — | $2T_{AIO\text{SYSCLK}}$ | — | ns |
| T_{LRPD} | BCLK rising edge to LRCK valid | — | — | $2T_{AIO\text{SYSCLK}}$ | — | |
| T_{SDS} | Set-up time SDATA input with regard to BCLK rising edge | — | — | $-3T_{AIO\text{SYSCLK}}^2$ | — | |
| T_{SDH} | Hold time SDATA Input with regard to BCLK rising edge | — | — | $4T_{AIO\text{SYSCLK}}^2$ | — | |
| F_{MCLK} | MCLK (not shown) output frequency | — | 6.144 | 24.576 | 49.152 | MHz |
| $DMCLK$ | MCLK output duty cycle | — | — | 50 | — | % |

1. BCLK may be inverted for more balanced setup and hold times.
2. Default AIO SYSCLK frequency is 400MHz.

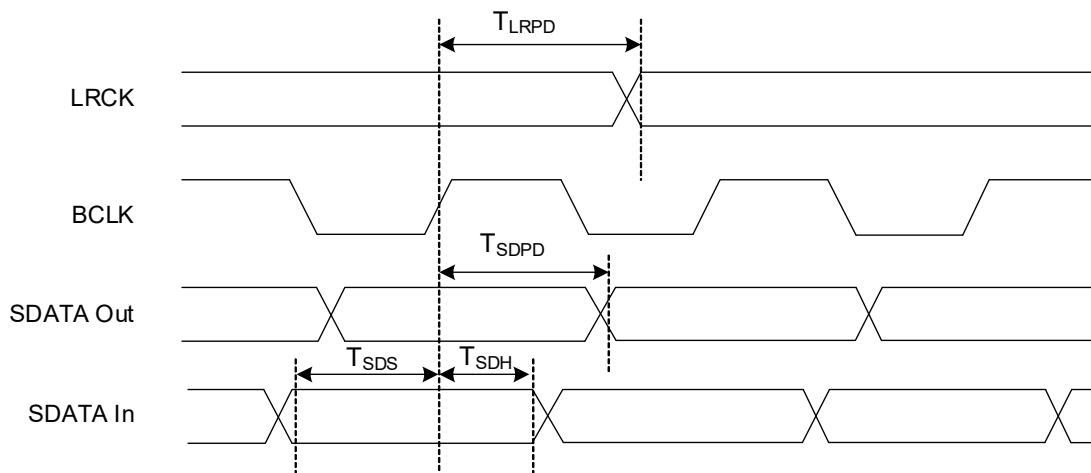


Figure 13. I2S Master Mode Timing

3.5.9.2. I2S Slave Mode Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 80. I2S Slave Mode Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|--|-----------|------|----------------------------|--------|-------|
| F_{BCLK} | BCLK Frequency | — | 16Fs | — | 64Fs | Hz |
| F_{BCLK_PCM} | BCLK Frequency in PCM Mono mode | — | 8Fs | — | 256Fs | |
| F_{BCLK_TDM} | BCLK Frequency in TDM mode | — | 16Fs | — | 256Fs | |
| F_s | — | — | 32 | — | 192 | kHz |
| D_{BCLK} | BCLK duty cycle | — | — | 50 | — | % |
| T_{LRS} | Setup time LRCK input with regard to BCLK active edge | — | — | $-3T_{AIO\text{SYSCLK}}^1$ | — | ns |
| T_{LRH} | Hold time LRCK input with regard to BCLK active edge | — | — | $4T_{AIO\text{SYSCLK}}^1$ | — | |
| T_{SDS} | Setup time SDATA Input with regard to BCLK active edge | — | — | $-3T_{AIO\text{SYSCLK}}^1$ | — | |
| T_{SDH} | Hold time SDATA Input with regard to BCLK active edge | — | — | $4T_{AIO\text{SYSCLK}}^1$ | — | |
| F_{MCLK} | MCLK (not shown) input frequency | — | — | 24.576 | 49.152 | MHz |
| D_{MCLK} | MCLK input duty cycle | — | — | 50 | — | % |

1. Default AIO SYSCLK frequency is 400MHz.

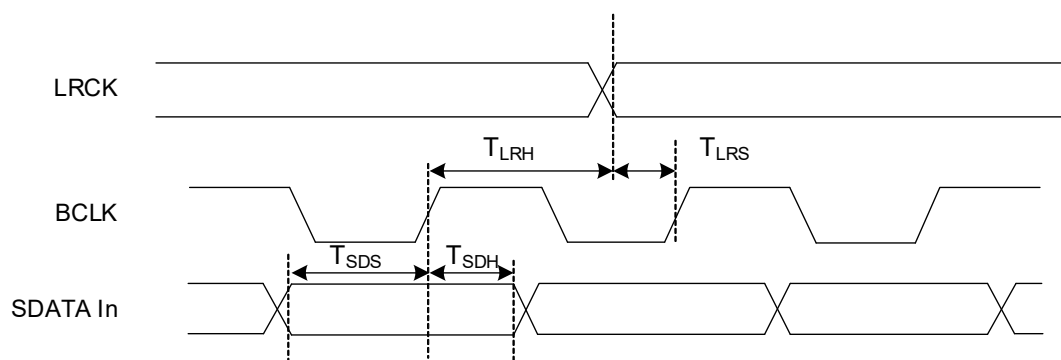


Figure 14. I2S Slave Mode Timing

3.5.10. Pulse-Width Modulation (PWM) Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 81. PWM Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------|---------------------------|------------------------|----------|-----|---------|-------|
| T _{PERIOD} | PWM | With 2-bit resolution | 20ns | – | 81.92μs | – |
| | | With 16-bit resolution | 655.35μs | – | 2.684s | – |
| – | PWM Duty Cycle | – | 0 | – | 100 | % |
| – | PWM Duty Cycle Resolution | – | 2 | – | 16 | bit |

3.5.11. ADC Inputs

3.5.11.1. ADC Electrical Information

(Over full range of values listed in the [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 82. ADC Electrical Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------------|--|-------|-----|------|-------|
| T _{OUT} | Digitalization Time | 0.11 | – | 20 | μs |
| V _{ADCIN_FS} | ADC_IN (analog input) full-scale voltage | – | – | 1.2 | V |
| – | Resolution | 6 | 12 | 12 | bits |
| INL | Integral Nonlinearity (INL) | – | – | ±2.2 | LSB |
| DNL | Differential Nonlinearity (DNL) | -0.97 | – | 1.9 | LSB |
| OSE | Offset error | – | – | ±0.7 | %FS |

3.5.12. USB 2.0 Timing

3.5.12.1. USB 2.0 DC Characteristics

(Over full range of values listed in Table 62, Recommended Operating Conditions unless otherwise specified.)

Table 83. USB 2.0 DC Electrical

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--|---|-------|-----|------|-------|
| V_{IH} | High (driven) | Note ¹ | 2.0 | – | – | V |
| V_{IHZ} | High (floating) | | 2.7 | – | 3.6 | |
| V_{IL} | Low | | – | – | 0.8 | |
| V_{DI} | Differential Input Sensitivity | $ (D+)-(D-) $ Note ¹ | 0.2 | – | – | |
| V_{CM} | Differential Common Mode Range | Includes VDI range Note ¹ | 0.8 | – | 2.5 | |
| Input Levels for High-speed: | | | | | | |
| V_{HSSQ} | High-speed squelch detection threshold (differential signal amplitude) | – | 100 | – | 150 | mV |
| V_{HSDSC} | High-speed disconnect detection threshold (differential signal amplitude) | – | 525 | – | 625 | |
| V_{HSCM} | High-speed data signaling common mode voltage range (guideline for receiver) | – | -50 | – | 500 | |
| Output Levels for Full-speed: | | | | | | |
| V_{OL} | Low | Note ¹ , Note ² | 0.0 | – | 0.3 | V |
| V_{OH} | High (Driven) | Note ¹ , Note ³ | 2.8 | – | 3.6 | |
| V_{OSE1} | SE1 | – | 0.8 | – | – | |
| V_{CRS} | Output Signal Crossover voltage | Note ⁴ | 1.3 | – | 2.0 | |
| Output Levels for High-speed: | | | | | | |
| V_{HSOI} | High-speed idle level | – | -10.0 | – | 10.0 | mV |
| V_{HSOH} | High-speed data signaling high | – | 360 | – | 440 | |
| V_{HSOL} | High-speed data signaling low | – | -10.0 | – | 10.0 | |
| V_{CHIRPJ} | Chirp J level (differential voltage) | – | 700 | – | 1100 | |
| V_{CHIRPK} | Chirp K level (differential voltage) | – | -900 | – | -500 | |
| Input Capacitance for Full-speed: | | | | | | |
| C_{IND} | Downstream Facing Port | Note ⁵ | – | – | 150 | pF |
| C_{INUB} | Upstream Facing Port (without cable) | Note ⁶ | – | – | 100 | |
| C_{EDGE} | Transceiver edge rate control capacitance | – | – | – | 75 | |

Table 83. USB 2.0 DC Electrical (Continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------------------|---|--------------|-------|-----|-------|-------|
| Terminations: | | | | | | |
| R _{PU} | Bus pull-up Resistor on Upstream facing port | 1.5 kohm ±5% | 1.425 | — | 1.575 | kohm |
| R _{PD} | Bus pull-down Resistor on Downstream Facing Port | 15 kohm ±5% | 14.25 | — | 15.75 | |
| Z _{INP} | Input impedance exclusive of pull-up/pull-down (for full-speed) | — | 300 | — | — | |
| V _{TERM} | Termination voltage for upstream facing port pull-up (R _{PU}) | — | 3.0 | — | 3.6 | V |
| Termination in High-speed: | | | | | | |
| V _{HSTERM} | Termination voltage in high-speed | — | -10 | — | 10 | mV |

1. Measured at A or B connector.
2. Measured with RL of 1.425 kohm to 3.6V.
3. Measured with RL of 14.25 kohm to GND.
4. Excluding the first transition from the idle state.
5. Measured at A receptacle.
6. Measured at B receptacle.

3.5.12.2. USB 2.0 Source Electrical Characteristics

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless otherwise specified.)

Table 84. USB High-speed Source Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------------------|--|-----------|----------|-----|------------------------|-------|
| Driver Characteristics: | | | | | | |
| T _{H_{SR}} | Rise Time (10%–90%) | — | 500 | — | — | ps |
| T _{H_{SF}} | Fall Time (10%–90%) | — | 500 | — | — | ps |
| Z _{H_{SDRV}} | Driver Output Resistance (which also serves as high speed termination) | — | 40.5 | — | 49.5 | ohm |
| Clock Timings: | | | | | | |
| T _{H_{SDRAT}} | High-speed Data Rate | — | 479.760 | — | 480.240 | Mbps |
| T _{H_{SFRAM}} | Microframe Interval | — | 124.9375 | — | 125.0625 | ms |
| T _{H_{SRFI}} | Consecutive Microframe Interval Difference | — | — | — | 4 high-speed bit times | — |

Table 85. USB Full-speed Source Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------------------|--|---|---------|-----|---------|-------|
| Driver Characteristics: | | | | | | |
| T_{FR} | Rise Time | — | 4 | — | 20 | ns |
| T_{FF} | Fall Time | — | 4 | — | 20 | ns |
| T_{FRFM} | Differential Rise and Fall Time Matching | T_{FR}/T_{FF} Note ¹ | 90 | — | 111.11 | % |
| Z_{DRV} | Driver Output Resistance for driver which is not high-speed capable. | — | 28 | — | 44 | ohm |
| Clock Timings: | | | | | | |
| $T_{FDRATHS}$ | Full-speed Data Rate for hubs and devices which are high speed capable. | Average bit rate | 11.9940 | — | 12.0060 | Mbps |
| T_{FDRATE} | Full-speed Data Rate for devices which are high-speed capable. | Average bit rate | 11.9700 | — | 12.0300 | Mbps |
| T_{FRAME} | Frame Interval | — | 0.9995 | — | 1.0005 | ms |
| T_{RFI} | Consecutive Frame Interval Jitter | No clock adjustment | — | — | 42 | ns |
| Full-speed Data Timings: | | | | | | |
| T_{DJ1} | Source Jitter Total (including frequency tolerance): To Next Transition | Note ¹ Note ² Note ³ | -3.5 | — | 3.5 | ns |
| T_{DJ2} | For Paired transitions | Note ⁴ | -4 | — | 4 | |
| T_{FDEOP} | Source Jitter for Differential Transition to SEO Transition | Note ³ | -2 | — | 5 | |
| T_{JR1} | Receiver jitter: To Next Transition | Note ³ | -18.5 | — | 18.5 | |
| T_{JR2} | For Paired Transitions | — | -9 | — | 9 | |
| T_{FEOPT} | Source SEO interval of EOP | — | 160 | — | 175 | |
| T_{FEOPR} | Receiver SEO interval of EOP | Note ⁵ | 82 | — | — | |
| T_{FST} | Width of SEO interval during differential transition | — | — | — | 14 | |

1. Excluding the first transition from the idle state.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. For both transitions of differential signaling.
5. Must accept as valid EOP.

3.5.13. PCIe Timing

For electrical specifications (2.5 and 5.0GT/s), refer to *PCI Express® Base Specification Revision 2.0*.

3.5.14. HDMI TX

3.5.14.1. HDMI TX DC Operating Conditions

(Over full range of values listed in Table 62, Recommended Operating Conditions unless specified.)

Table 86. HDMI TX DC Operating Conditions for HDMI 1.4b

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|---|---|---------------|-----|---------------|-------|
| V_{OFF} | Single-ended standby (off) output voltage | — | $AV_{CC}-10$ | — | $AV_{CC}+10$ | mV |
| V_{SWING} | Single-ended output swing voltage | — | 400 | — | 600 | |
| V_H | Single-ended high level output voltage | If attached Sink supports only ≤ 165 MHz | $AV_{CC}-10$ | — | $AV_{CC}+10$ | |
| | | If attached Sink supports > 165 MHz | $AV_{CC}-200$ | — | $AV_{CC}+10$ | |
| V_L | Single-ended low level output voltage | If attached Sink supports only ≤ 165 MHz | $AV_{CC}-600$ | — | $AV_{CC}-400$ | |
| | | If attached Sink supports > 165 MHz | $AV_{CC}-700$ | — | $AV_{CC}-400$ | |

Table 87. HDMI TX DC Characteristics for $3.4\text{Gbps} < R_{bit} \leq 6.0\text{Gbps}$ at TP1

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|---|-----------|----------------|-----|---------------|-------|
| V_{SWING} | Single-ended output swing voltage: Data channels 0, 1, 2 | — | 400 | — | 600 | mV |
| | Single-ended output swing voltage: Clock channel | — | 200 | — | 600 | |
| V_H | Single-ended high level output voltage: Data channels 0, 1, 2 | — | $AV_{CC}-400$ | — | $AV_{CC}+10$ | |
| | Single-ended high level output voltage: Clock channel | — | $AV_{CC}-400$ | — | $AV_{CC}+10$ | |
| V_L | Single-ended low level output voltage: Data channels 0, 1, 2 | — | $AV_{CC}-1000$ | — | $AV_{CC}-400$ | |
| | Single-ended low level output voltage: Clock channel | — | $AV_{CC}-1000$ | — | $AV_{CC}-200$ | |

3.5.14.2. HDMI TX AC Operating Conditions

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 88. HDMI TX AC Operating Conditions for 1.4b

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-------------------------------------|-----------|-----|-----|------|-----------------|
| — | Rise time / fall time (20%-80%) | — | 75 | — | — | ps |
| — | Intra-Pair Skew at Source Connector | — | — | — | 0.15 | T_{bit} |
| — | Inter-Pair Skew at Source Connector | — | — | — | 0.20 | $T_{character}$ |
| — | Clock duty cycle | — | 40 | 50 | 60 | % |
| — | TMDS Differential Clock Jitter | — | — | — | 0.25 | T_{bit} |

Table 89. HDMI TX AC Characteristics for $3.4\text{Gbps} < R_{bit} \leq 6.0\text{Gbps}$ at TP1

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|---|-----------|------|-----|------|-----------------|
| — | Rise time / fall time (20%-80%): Data channels 0, 1, 2 | — | 42.5 | — | — | ps |
| — | Rise time / fall time (20%-80%): Clock Channel | — | 75 | — | — | ps |
| — | Intra-Pair Skew at Source Connector | — | — | — | 0.15 | T_{bit} |
| — | Inter-Pair Skew at Source Connector | — | — | — | 0.20 | $T_{character}$ |
| — | Clock duty cycle | — | 40 | 50 | 60 | % |
| — | TMDS Differential Clock Jitter | At TP2_EQ | — | — | 0.30 | T_{bit} |

3.5.15. HDMI RX

3.5.15.1. HDMI RX DC Operating Conditions

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 90. HDMI RX DC Operating Conditions at TP2 (for reference only)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|--|---------------------------------|---------------|-----|----------------|-------|
| V_{idiff} | Input Differential Voltage Level | – | 150 | – | 1200 | mV |
| V_{icm1} | Input Common Mode Voltage | Sink supports >165 MHz | $AV_{cc}-400$ | – | $AV_{cc}-37.5$ | |
| V_{icm2} | Input Common Mode Voltage (AC coupled) | – | $AV_{cc}-10$ | – | $AV_{cc}+10$ | |
| – | Differential Voltage Level | Source disabled or disconnected | $AV_{cc}-10$ | – | $AV_{cc}+10$ | |

3.5.15.2. HDMI RX AC Operating Conditions

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Table 91. HDMI RX AC Operating Conditions at TP2 (for reference only)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|---|--|-------------------------|-----|------|-----------|
| – | Minimum differential sensitivity | – | – | – | 150 | mV |
| – | Maximum differential input | – | 1560 | – | – | mV |
| – | Max allowable Intra-pair Skew at Sink connector | For TMDS Clock rates 222.75MHz and below | 0.4 | – | – | T_{bit} |
| | | For TMDS Clock rates above 222.75MHz | $0.15T_{bit}+112$ | – | – | ps |
| – | Max allowable Inter-pair Skew at Sink connector | – | $0.2T_{character}+1.78$ | – | – | ns |
| – | TMDS Clock Jitter | See HDMI spec for conditions | – | – | 0.30 | T_{bit} |

3.5.16. LPDDR4 Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

Refer to JESD209-4A for LPDDR4 SDRAM specification.

3.5.17. eMMC Timing

(Over full range of values listed in [Table 62, Recommended Operating Conditions](#) unless specified.)

3.5.17.1. eMMC Timing - Default Bus

Table 92. eMMC Timing - Default Bus

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--------------------------------------|-----------|-------------------|-----|------|-------|
| f_{PP} | Clock Frequency Data Transfer Mode 3 | — | 0 | — | 26 | MHz |
| f_{OD} | Clock Frequency Identification Mode | — | 0 | — | 400 | kHz |
| t_{WL} | Clock Low time | — | 10 | — | — | ns |
| t_{WH} | Clock High time | — | 10 | — | — | |
| t_{TLH} | Clock Rise time | — | 0.4 | — | 1.32 | |
| t_{THL} | Clock Fall time | — | 0.4 | — | 1.32 | |
| Inputs DAT (referenced to Clock): | | | | | | |
| t_{ISU} | Input Setup time | — | Note ¹ | — | — | ns |
| t_{IH} | Input Hold time | — | Note ¹ | — | — | |
| Outputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ODLY} | Output Delay time | — | Note ¹ | — | — | ns |

1. Refer to *JEDEC Standard No. 84-B51* for eMMC timing specifications.

3.5.17.2. eMMC Timing - High-Speed Bus

Table 93. eMMC Timing - High-Speed Bus

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--------------------------------------|--------------------|-------------------|-----|------|-------|
| f_{PP} | Clock Frequency Data Transfer Mode 3 | — | 0 | — | 52 | MHz |
| f_{OD} | Clock Frequency Identification Mode | — | 0 | — | 400 | kHz |
| t_{WL} | Clock Low time | — | — | — | — | ns |
| t_{WH} | Clock High time | — | — | — | — | |
| t_{TLH} | Clock Rise time | — | 0.4 | — | 1.32 | |
| t_{THL} | Clock Fall time | — | 0.4 | — | 1.32 | |
| Inputs DAT (referenced to Clock): | | | | | | |
| t_{ISU} | Input Setup time | — | Note ¹ | — | — | ns |
| t_{IH} | Input Hold time | — | Note ¹ | — | — | |
| Outputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ODLY} | Output Delay time | Data Transfer Mode | Note ¹ | — | — | ns |
| t_{RISE} | Signal Rise time | — | 0.4 | — | 1.32 | |
| t_{FALL} | Signal Fall time | — | 0.4 | — | 1.32 | |

1. Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

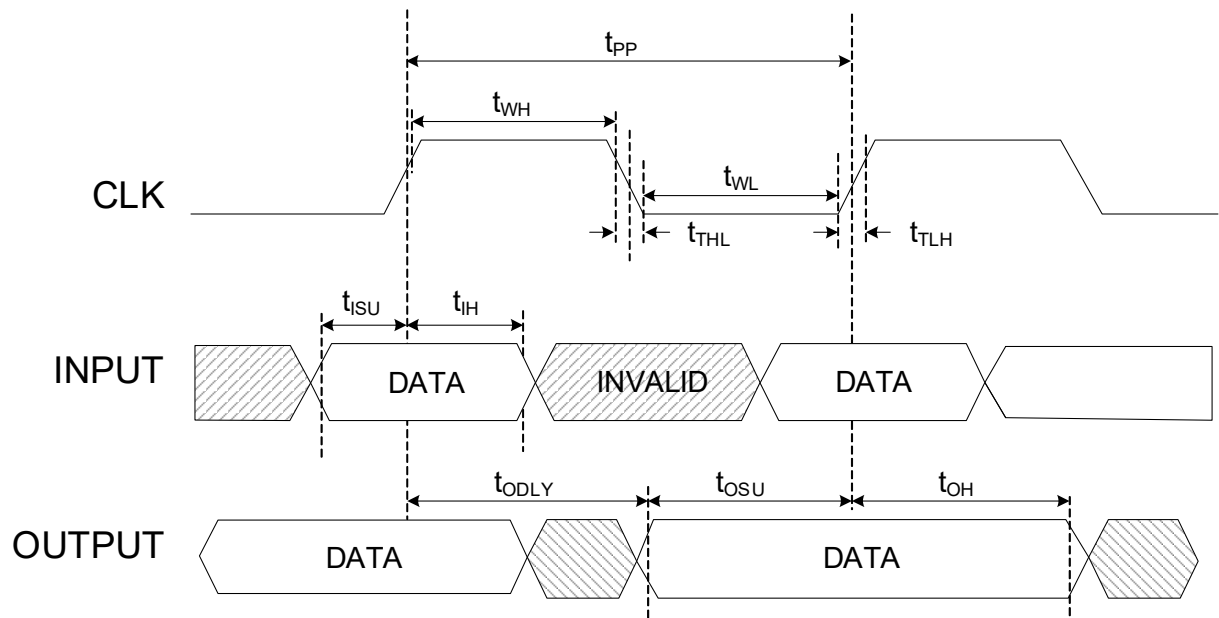


Figure 15. eMMC Timing - Default Bus and High-Speed Bus Interface Timing

Note: Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

3.5.17.3. eMMC Timing - High-Speed Dual Rate Bus

Table 94. eMMC Timing - High-Speed Dual Rate Bus

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--------------------|--------------------|-------------------|-----|------|-------|
| — | Clock Frequency | — | 45 | — | 55 | MHz |
| Inputs DAT (referenced to Clock): | | | | | | |
| t_{ISU} | Input Setup time | — | Note ¹ | — | — | ns |
| t_{IH} | Input Hold time | — | Note ¹ | — | — | |
| Outputs CMD, DAT (referenced to Clock): | | | | | | |
| t_{ODLY} | Output Clock Delay | Data Transfer Mode | Note ¹ | — | — | ns |
| t_{RISE} | Signal Rise Time | — | 0.4 | — | 1.32 | |
| t_{FALL} | Signal Fall Time | — | 0.4 | — | 1.32 | |

1. Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

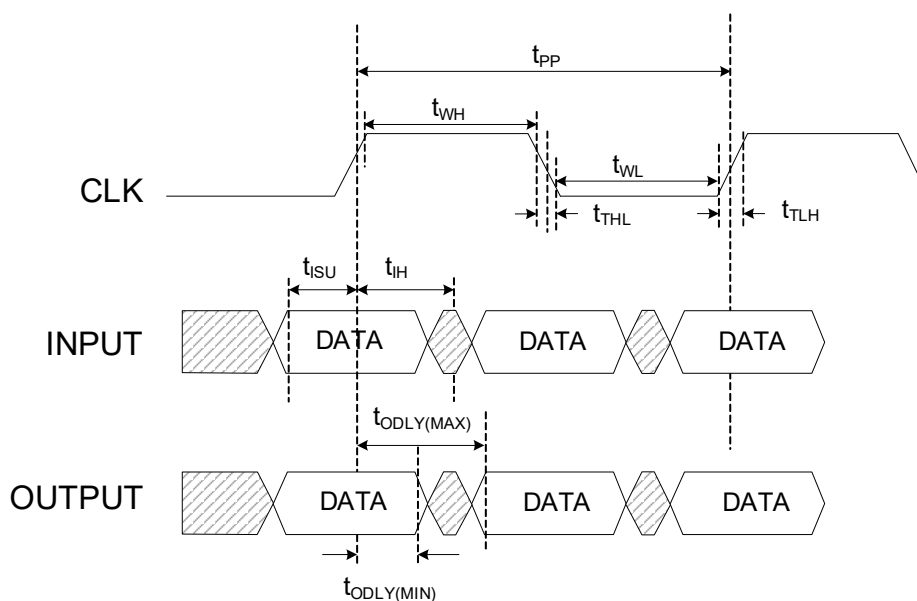


Figure 16. eMMC Timing - High-Speed Dual Rate Interface Timing

3.5.17.4. eMMC Timing - HS200 Mode & HS400 Mode

Refer to JEDEC Standard No. 84-B51 for eMMC timing specifications.

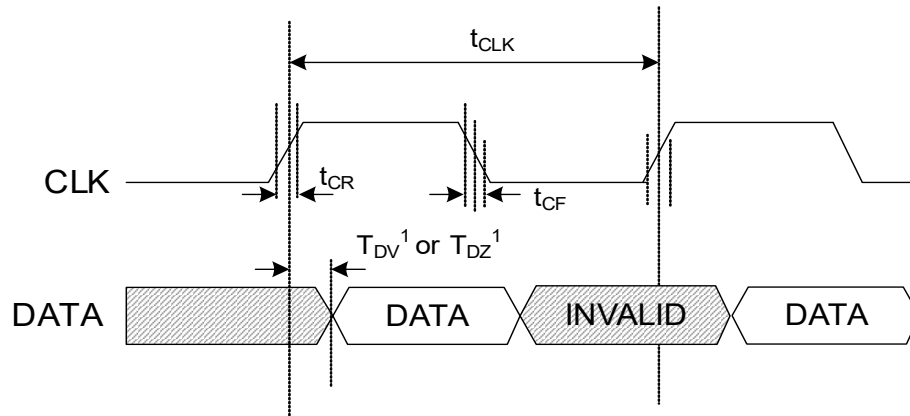
3.5.18. Pulse Density Modulation

Table 95. Pulse Density Modulation (Classic PDM) Timing Parameters - SDR Mode

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------|-----------------------|-----------|-----|-----|----------------------------|-------|
| f_{CLK}^1 | PDM Clock Frequency | — | — | — | $F_{\text{AIOSYSCLK}}/4^2$ | MHz |
| t_{D} | Clock Duty Cycle | — | — | 50 | — | % |
| t_{CR} | Input Clock Rise Time | 10 - 90% | — | — | $T_{\text{AIOSYSCLK}}^2$ | ns |
| t_{CF} | Input Clock Fall Time | 90 - 10% | — | — | $T_{\text{AIOSYSCLK}}^2$ | ns |

1. $f_{\text{CLK}} = 1/t_{\text{CLK}}$

2. Default $F_{\text{AIOSYSCLK}}$ is 400MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

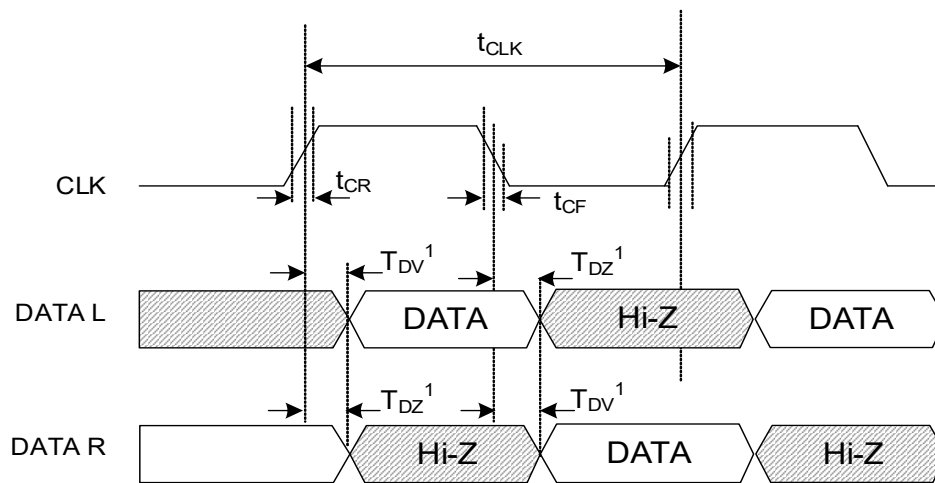
Figure 17. PDM Timing - SDR Mode

Table 96. Pulse Density Modulation (Half Cycle PDM) Timing Parameters - DDR Mode

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|-----------------------|-----------|-----|-----|---------------------|-------|
| f_{CLK}^1 | PDM Clock Frequency | — | — | — | $F_{AIOSYSCLK}/4^2$ | MHz |
| t_D | Clock Duty Cycle | — | — | 50 | — | % |
| t_{CR} | Input Clock Rise Time | 10 - 90% | — | — | $T_{AIOSYSCLK}^2$ | ns |
| t_{CF} | Input Clock Fall Time | 90 - 10% | — | — | $T_{AIOSYSCLK}^2$ | ns |

1. $f_{CLK} = 1/t_{CLK}$

2. Default $F_{AIOSYSCLK}$ is 400MHz.



1. PDM data sampling point is configurable across the t_{CLK} period.

Figure 18. PDM Timing - DDR Mode

3.5.19. MIPI DSI Characteristics

3.5.19.1. Input DC Specifications

Table 97 describes the Input DC Specifications.

Table 97. Input DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------------------------|---|--|-------|-----|------|---------|
| Apply to DATAOP/N Inputs: | | | | | | |
| V_I | Input signal voltage range | — | -50 | — | 1350 | mV |
| I_{LEAK} | Input leakage current | $V_{GNDSH(min)} \leq V_I \leq V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode | -10 | — | 10 | μ A |
| V_{GNDSH} | Ground shift | — | -50 | — | 50 | mV |
| $V_{OH(absmax)}$ | Transient pin voltage level | — | -0.15 | — | 1.45 | V |
| $t_{VOH(absmax)}$ | Maximum transient time above $V_{OH(absmax)}$ | — | — | — | 20 | ns |

3.5.19.2. MIPI DSI HS Line Drivers DC Specifications

Table 98. MIPI DSI HS Line Drivers DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------------|---|--------------------------------------|-----|-----|------|----------|
| $ V_{OD} $ | HS Transmit Differential output voltage magnitude | $80 \Omega \leq R_L \leq 125 \Omega$ | 140 | 200 | 270 | mV |
| $\Delta V_{OD} $ | Change in Differential output voltage magnitude between logic states | $80 \Omega \leq R_L \leq 125 \Omega$ | — | — | 14 | |
| V_{CMTX} | Steady-state common-mode output voltage | $80 \Omega \leq R_L \leq 125 \Omega$ | 150 | 200 | 250 | |
| $\Delta V_{CMTX(1,0)}$ | Changes in steady-state common-mode output voltage between logic states | $80 \Omega \leq R_L \leq 125 \Omega$ | — | — | 5 | |
| V_{OHHS} | HS output high voltage | $80 \Omega \leq R_L \leq 125 \Omega$ | — | — | 360 | |
| Z_{OS} | Single-ended output impedance | — | 40 | 50 | 62.5 | Ω |
| ΔZ_{OS} | Single-ended output impedance mismatch | — | — | — | 10 | % |

3.5.19.3. MIPI DSI LP Line Drivers DC Specifications

Table 99. MIPI DSI LP Line Drivers DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------------------|---|-----------|-----|-----|-----|----------|
| V_{OL} | Output low-level SE voltage | — | -50 | — | 50 | mV |
| V_{OH} | Output high-level SE voltage | — | 1.1 | 1.2 | 1.3 | V |
| Z_{OLP} | Single-ended output impedance | — | 110 | — | — | Ω |
| $\Delta Z_{OLP(01,10)}$ | Single-ended output impedance mismatch driving opposite level | — | — | — | 20 | % |
| $\Delta Z_{OLP(00,11)}$ | Single-ended output impedance mismatch driving same level | — | — | — | 5 | % |

3.5.19.4. MIPI DSI LP Line Receiver DC Specifications

Table 100. MIPI DSI LP Line Receiver DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|--------------------------------|-----------|-----|-----|-----|-------|
| V_{IL} | Input low voltage, not in ULPS | — | — | — | 550 | mV |
| $V_{IL-ULPS}$ | Logic 0 input voltage, ULPS | — | — | — | 300 | |
| V_{IH} | Input high voltage | — | 740 | — | — | |
| V_{HYST} | Input hysteresis | — | 25 | — | — | |

3.5.19.5. MIPI DSI Contention Line Receiver DC Specifications

Table 101. MIPI DSI Contention Line Receiver DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------|----------------------------|-----------|-----|-----|-----|-------|
| V_{ILF} | Input low fault threshold | — | — | — | 200 | mV |
| V_{IHF} | Input high fault threshold | — | 450 | — | — | |

3.5.19.6. MIPI DSI Clock Signal and Data-Clock Timing Specifications

Table 102. MIPI DSI Clock Timing

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--------------|--|------|-----|------|-------|---|
| — | Maximum Serial Data rate (forward direction) | 80 | — | 2500 | Mbps | Condition: On DATAP/N outputs. $80 \Omega \leq R_L \leq 125 \Omega$ |
| F_{DDRCLK} | DDR CLK frequency | 40 | — | 1250 | MHz | Condition: On CLKP/N outputs. |
| T_{DDRCLK} | DDR CLK period | 0.8 | — | 25 | ns | Condition: $80 \Omega \leq R_L \leq 125 \Omega$ |
| UI_{INST} | UI instantaneous | 0.4 | — | 12.5 | ns | The Max value corresponds to a minimum Mbps data rate. |
| ΔUI | UI variation | -10% | — | 10% | UI | — |
| t_{CDC} | DDR CLK duty cycle | — | 50 | — | % | Condition: $t_{CDC} = t_{CPH} / T_{DDRCLK}$ |
| t_{CPH} | DDR CLK high time | — | 1 | — | UI | — |
| t_{CPL} | DDR CLK low time | — | 1 | — | UI | — |

3.5.19.7. MIPI DSI HS Line Drivers AC Specifications

Table 103. MIPI DSI HS Line Drivers AC Specifications

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--------|--------------------------------------|-----|-----|------|-------|---|
| t_r | Differential output signal rise time | — | — | 0.30 | UI | Condition: 20% to 80%, $R_L = 50 \Omega$ For PHY operating at or below 1Gbps |
| | | — | — | 0.35 | UI | For PHY operating above 1Gbps and below or at 1.5Gbps |
| | | 100 | — | — | ps | For PHY operating below or at 1.5Gbps |
| t_f | Differential output signal fall time | — | — | 0.30 | UI | Condition: 20% to 80%, $R_L = 50 \Omega$ For PHY operating at or below 1Gbps |
| | | — | — | 0.35 | UI | For PHY operating above 1Gbps and below or at 1.5Gbps |
| | | 100 | — | — | ps | For PHY operating below or at 1.5Gbps |

3.5.19.8. MIPI DSI LP Line Driver and Receiver AC Specifications

For MIPI DSI LP line driver and receiver AC specifications, refer to the *MIPI D-PHY Specification v2*.

3.5.20. MIPI CSI Characteristics

3.5.20.1. Input DC Specifications

Table 104. Input DC Specifications

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--|---|-------|-----|------|---------|--|
| Apply to CLKP/N and DATAP/N Inputs: | | | | | | |
| V_{PIN} | Pin signal voltage range | -50 | — | 1350 | mV | — |
| I_{LEAK} | Pin leakage current | -10 | — | 10 | μ A | $V_{GNDSH(min)} \leq V_{PIN} \leq V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP receive mode |
| V_{GNDSH} | Ground shift | -50 | — | 50 | mV | — |
| $V_{PIN(absmax)}$ | Transient pin voltage level | -0.15 | — | 1.45 | V | — |
| $V_{PIN(absmax)}$ | Maximum transient time above $V_{OH(absmax)}$ | — | — | 20 | ns | The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations the voltage overshoot and undershoot must stay within the V_{PIN} range. |

3.5.20.2. HS Line Receiver DC Specifications

Table 105. HS Line Receiver DC Specifications

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|--------------|---|-----|-----|-----|---|--|
| V_{IDTH} | Differential input high voltage threshold | — | — | 70 | mV | D-PHY spec 1.1 compatibility mode (≤ 1.5 Gbps) |
| | | — | — | 40 | | In case of High-speed deskew calibration (> 1.5 Gbps) |
| V_{IDTL} | Differential input low voltage threshold | -70 | — | — | | D-PHY spec 1.1 compatibility mode (≤ 1.5 Gbps) |
| | | -40 | — | — | | In case of High-speed deskew calibration (> 1.5 Gbps) |
| V_{IHHS} | Single ended input high voltage | — | — | 460 | | Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz. |
| V_{ILHS} | Single ended input low voltage | -40 | — | — | | |
| V_{CMRXDC} | Input common mode voltage | 70 | — | 330 | Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz. | |
| Z_{ID} | Differential input impedance | 80 | 100 | 125 | Ω | — |

3.5.20.3. LP Line Drivers DC Specifications

Table 106 describes the LP Line Drivers DC Specifications.

Table 106. LP Line Drivers DC Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|-------------------------------|-----|-----|-----|----------|
| V_{OL} | Output low-level SE voltage | -50 | — | 50 | mV |
| V_{OH} | Output high-level SE voltage | 1.1 | 1.2 | 1.3 | V |
| Z_{OLP} | Single-ended output impedance | 110 | — | — | Ω |

3.5.20.4. LP Line Receiver DC Specifications

Table 107 describes the LP Line Receiver DC Specifications.

Table 107. LP Line Receiver DC Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|---------------|-----------------------------|-----|-----|-----|-------|
| V_{IL} | Input low voltage | — | — | 550 | mV |
| V_{IH} | Input high voltage | 740 | — | — | mV |
| $V_{IL-ULPS}$ | Logic 0 input voltage, ULPS | — | — | 300 | mV |
| V_{HYST} | Input hysteresis | 25 | — | — | mV |

3.5.20.5. Contention Line Receiver DC Specifications

Table 108 describes the Contention Line Receiver DC Specifications.

Table 108. Contention Line Receiver DC Specifications

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|----------------------------|-----|-----|-----|-------|
| V_{ILF} | Input low fault threshold | — | — | 200 | mV |
| V_{IHF} | Input high fault threshold | 450 | — | — | mV |

3.5.20.6. MIPI CSI Clock Signal and Data-Clock Timing Specifications

Table 109. High Speed Clock Timings

| Symbol | Parameter | Condition | Min | Typ | Max | Units | Notes |
|-------------------------------|--|---|-------|-----|------|-------------|---|
| — | Maximum Serial Data rate (forward direction) | On DATAP/N outputs. $80 \Omega \leq R_L \leq 125 \Omega$ | 80 | — | 2500 | Mbps | |
| F _{DDRCLK} | DDR CLK frequency | On CLKP/N outputs | 40 | — | 1250 | MHz | |
| T _{DDRCLK} | DDR CLK period | $80 \Omega \leq R_L \leq 125 \Omega$ | 0.8 | — | 25 | ns | |
| U _{IINST} | UI instantaneous | — | 0.4 | — | 12.5 | ns | This value corresponds to a minimum Mbps data rate. |
| t _{CDC} | DDR CLK duty cycle | $t_{CDC} = t_{CPH} / T_{DDRCLK}$ | — | 50 | — | % | |
| t _{CPH} | DDR CLK high time | — | — | 1 | — | UI | |
| t _{CPL} | DDR CLK low time | — | — | 1 | — | UI | |
| — | DDR CLK / DATA Jitter | — | — | 75 | — | ps pk-pk | When UI < 1ns, within a single burst. |
| T _{SETUP[RX]} | Data to Clock Setup Time (RX) | — | 0.15 | — | — | UI | For PHY operating at or below 1Gbps |
| | | — | 0.20 | — | — | | For PHY operating above 1Gbps and below or at 1.5Gbps |
| T _{HOLD[RX]} | Data to Clock Hold Time (RX) | — | 0.15 | — | — | | For PHY operating at or below 1Gbps |
| | | — | 0.20 | — | — | | For PHY operating above 1Gbps below or at 1.5Gbps |
| T _{SKEW[RX] static} | Static Data to Clock Skew RX Tolerance | — | -0.30 | — | 0.30 | | For PHY operating above 1.5Gbps and below or at 2.5Gbps |
| T _{SKEW[RX] dynamic} | Dynamic Data to Clock Skew Window RX Tolerance | — | 0.50 | — | — | | For PHY operating above 1.5Gbps and below or at 2.5Gbps |

3.5.20.7. MIPI CSI LP Line Drivers AC Specifications

For MIPI CSI LP Line Drivers AC Specifications, refer to the *MIPI D-PHY Specification v2*.

3.5.20.8. MIPI CSI LP Line Receivers AC Specifications

For MIPI CSI LP Line Receivers AC Specifications, refer to the *MIPI D-PHY Specification v2*.

4. Mechanical Drawing

4.1. SL1680 Package Drawing

Note: The drawings in [Figure 19](#), [Figure 20](#), and [Figure 21](#) are not to scale.

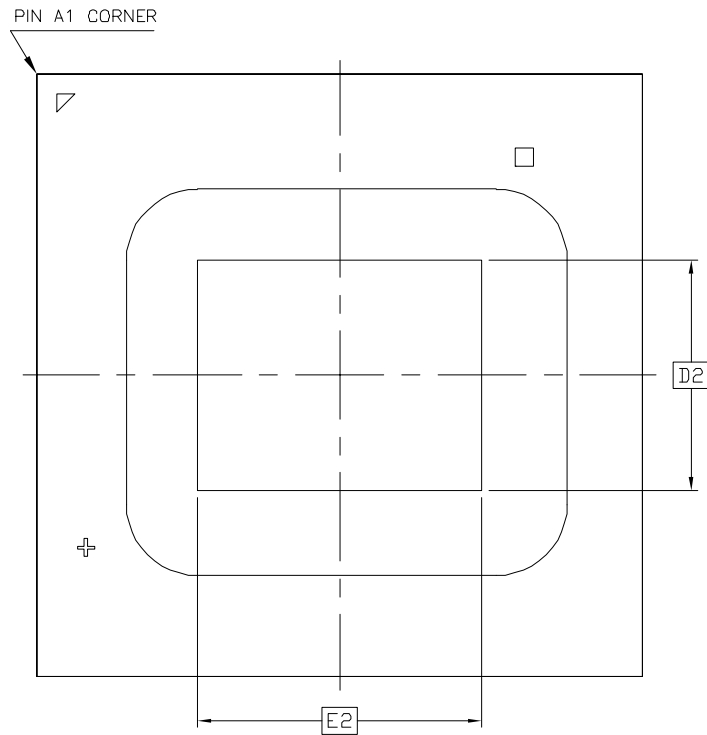


Figure 19. SL1680 Top View

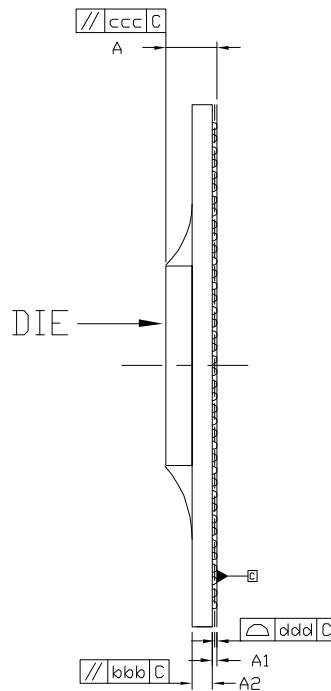


Figure 20. SL1680 Side View

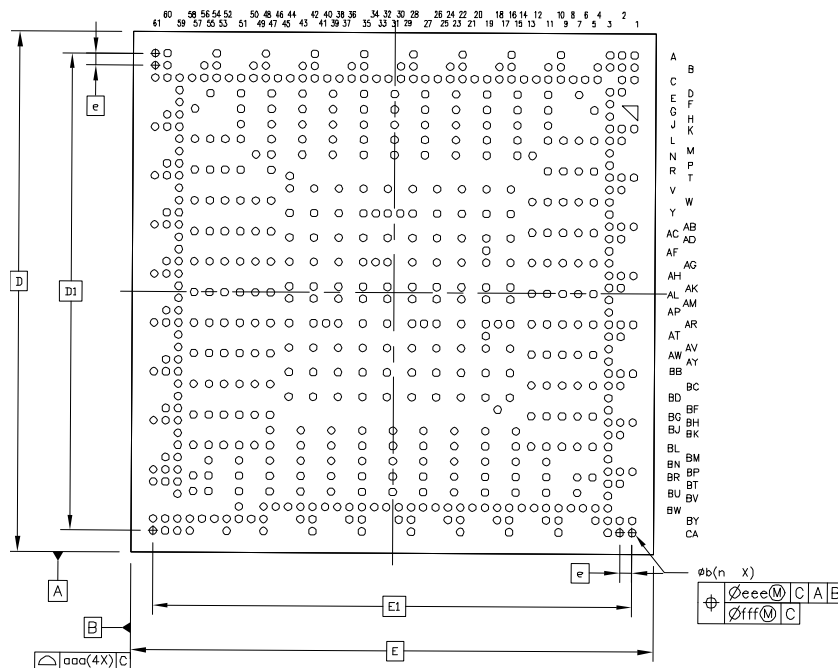


Figure 21. SL1680 Bottom View

Table 110. SL1680 Dimensions (in mm)

| | Symbol | Common Dimensions | | |
|--|--------|-------------------|-------|-------|
| | | Min | Typ | Max |
| Total Thickness | A | 1.585 | 1.692 | 1.799 |
| Stand Off | A1 | 0.110 | 0.160 | 0.210 |
| Substrate Thickness | A2 | 0.662 REF | | |
| Thickness from Substrate Surface to Die Backside | A3 | 0.870 REF | | |
| Body Size | D | 17.000 BSC | | |
| | E | 17.000 BSC | | |
| Ball Diameter | | 0.250 | | |
| Ball Width | b | 0.200 | 0.250 | 0.300 |
| Ball Pitch | e | 0.400 BSC | | |
| Ball Count | n | 605 | | |
| Edge Ball Center to Center | D1 | 15.600 BSC | | |
| | E1 | 15.600 BSC | | |
| Expose Die Size | D2 | 6.520 BSC | | |
| | E2 | 7.980 BSC | | |
| Package Edge Tolerance | aaa | 0.150 | | |
| Substrate Parallelism | bbb | 0.200 | | |
| Top Parallelism | ccc | 0.250 | | |
| Coplanarity | ddd | 0.080 | | |
| Ball Offset (Package) | eee | 0.150 | | |
| Ball Offset (Ball) | fff | 0.050 | | |

5. Part Order Numbering / Package Marking

5.1. Part Order Numbering

Table 111 provides a list of the available options for ordering.

Table 111. SL1680 Part Order Options

| Package Type | Part Number | Grade | Featured Option | Note |
|---------------|-------------------------|------------|-----------------|-----------------------|
| 605-pin FCBGA | SL1680A1-BYKXSZZ-T000-T | Consumer | Fully featured | Available now. |
| | SL1680A1-BYKXSYY-T000-T | | HDMI disabled | |
| | SL1680A1-BYKXSZZ-H000-T | Industrial | Fully featured | Available in Q3 2024. |
| | SL1680A1-BYKXSYY-H000-T | | HDMI disabled | Available in Q3 2024. |

5.2. Package Marking

Figure 22 shows a sample package marking and pin 1 location for the SL1680 device.



Figure 22. Package Marking and Pin 1 Location

6. References

- *SL1680 Embedded IoT Processor Functional Description* (PN: 505-001414-01)
Provides a functional description of the SL1680 device core.
- *Synaptics General Guide for Soldering SMD to PC Boards Application Note* (PN: 506-001443-01)
- *Synaptics General ESD/EOS Control Methods Application Note* (PN: 506-001454-01)
- MIPI D-PHY Specification v2.
- PV Compensation Application Note.
- PCI Express[®] Base Specification Revision 2.0
- JESD209-4A Specification.
- JESD51-12.01 Specification.

7. Revision History

| Last Modified | Revision | Description |
|---------------|----------|---|
| March 2024 | A | Release to production. |
| April 2024 | B | Update Section, Part Order Numbering, on page 92 . |
| August 2024 | C | <ul style="list-style-type: none"> Update availability for SL1680A1-BYKXSYY-H000-T in Table 111, SL1680 Part Order Options, on page 92. Add metadata keywords. |
| November 2024 | D | Corrected missing titles for the following tables: <ul style="list-style-type: none"> Table 10, USB3.0 Interface Table 11, HDMI Receiver PHY Interface Table 12, HDMI Transmitter PHY Interface Table 31, PCIe Interface Table 32, RGMII Interface Table 40, MIPI Camera Serial Interface (CSI1) Pins Table 59, RGMII Group Multiplexing Table 110, SL1680 Dimensions (in mm) |

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