SYN20708 Datasheet

Dual-Radio Bluetooth 5.4 and IEEE 802.15.4

1.1. Description

The Synaptics SYN20708 is a multiprotocol, dual- radio Bluetooth 5.4 system on a chip (SoC) that supports the Bluetooth Classic, Bluetooth Low Energy, Zigbee, Thread, and Matter protocols. The SYN20708 has two BT/BLE/IEEE 802.15.4 cores that can simultaneously function as either a receiver or transmitter. It supports concurrent BT/BLE and IEEE 802.15.4 (Thread and Zigbee) operation on both cores. The SYN20708 also integrates an Arm Cortex-M4 CPU running at 160 MHz and has a high-speed UART interface for connection with an external host processor.

1.2. Features

1.2.1. Key Features

- Complies with BT Core Specification Version 5.4 with support for future 6.0 specifications such as high accuracy distance measurement (HADM).
- Supports two 2.4 GHz band radios concurrently.
- Supports Bluetooth Class 1 and Class 2 TX operation.
- Supports Electronic Shelf Label (ESL).
- Supports HADM/channel sounding (BT 6.0 compliance expected).
- Supports BLE-LR, angle of departure (AoD), angle of arrival (AoA), and HW-capable ISOC.

1.2.2. Interfaces

- High-speed UART.
- Synaptics-proprietary Serial Enhanced Coexistence Interface (SECI) for Wi-Fi and BT coexistence.
- 3-wire IEEE 802.15.2 coexistence interface for Wi-Fi and BT coexistence.
- Optional Serial Peripheral Interface (SPI) for direct connection with local external flash.
- I^2C master to control external sensors.
- Debug UART.

1.2.3. General Features

- Fabricated using a 16 nm FinFET Compact (16FFC) process.
- Supports BLE Zephyr open-source software stack.
- Supports IEEE 802.15.4 (OpenThread and ZBOSS) up to version 2.
- Contains integrated 2.4 GHz power amplifiers and low-noise amplifiers.
- Supports external 2.4 GHz power amplifiers.
- Contains integrated Transmit/Receive (TR) switch.
- Supports external TR switch.
- Supports firmware download over UART for shared flash with a host processor, or from local, dedicated serial flash over an SPI.

- Four GPIO and antenna-selection pins for AoD and AoA determination or HADM (channel sounding).
- Supports secure boot.
- Package: 103-pin FCBGA,
  5.5 mm × 5.5 mm, 0.4 mm pitch.

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Contents

1.Introduction

1.1.System Overview

Figure 1 shows a SYN20708 functional block diagram.

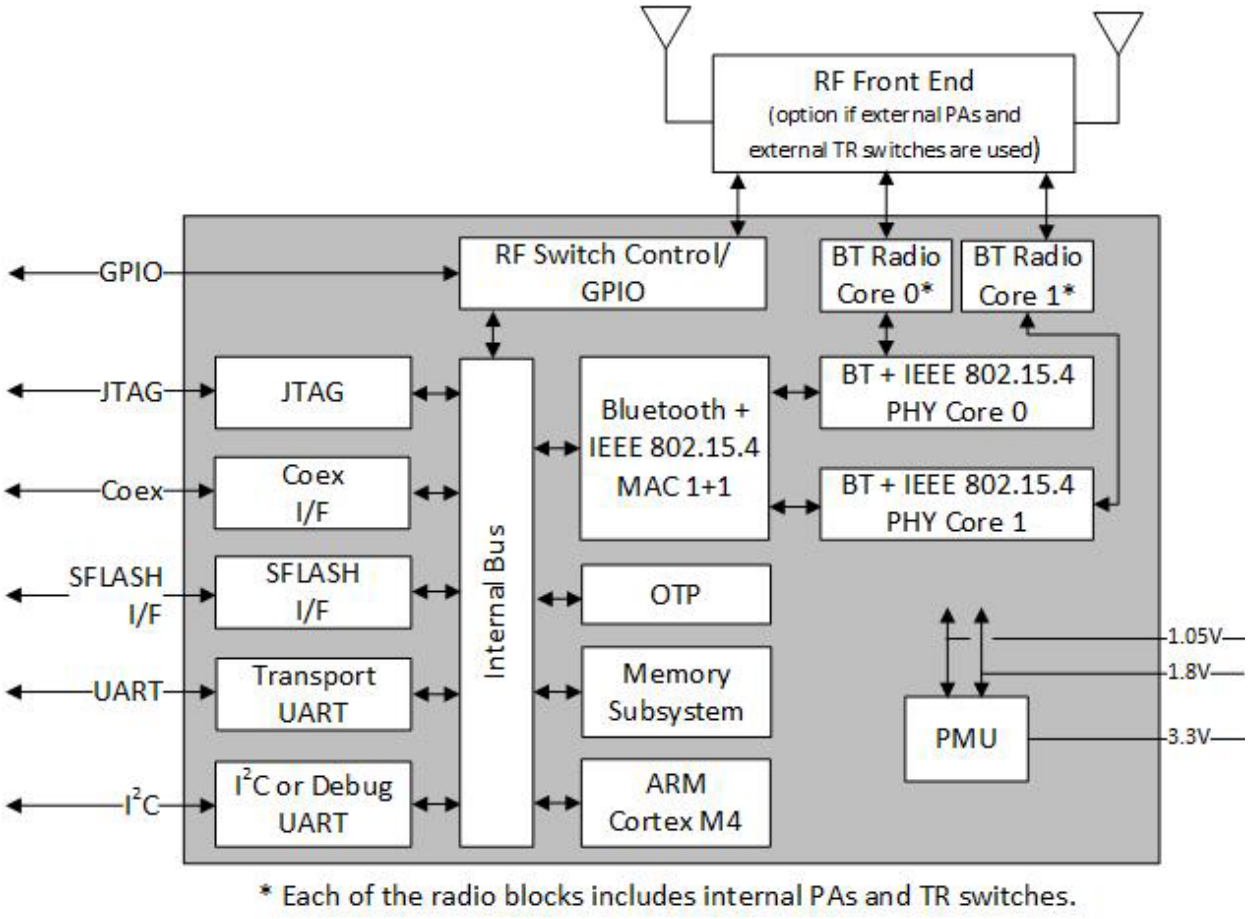

Figure 1. SYN20708 functional block diagram

1.2.Bluetooth and IEEE 802.15.4 System Overview

The BT system is a dual-radio Bluetooth 5.4+ compliant baseband processor and 2.4 GHz transceiver. It also has tightly-coupled support for IEEE 802.15.4 (Thread, Zigbee, etc.) using the 2.4 GHz Bluetooth radio.

1.2.1.Standards Support

The BT system supports all mandatory SIG BT 5.4+ features. In addition, it supports ranging technologies such as high-accuracy distance measurement (HADM), which is expected to be included in Bluetooth standards greater than BT 5.4+. The SYN20708 also supports worldwide

regulatory requirements and the latest publicly-available revisions of the Thread, Zigbee, and Matter standards.

1.2.2. Interfaces

The Bluetooth system supports a standard Host Controller Interface (HCI) via a high-speed UART. It also supports a coexistence interface.

1.2.3. Processor and Memory

The BT system includes an Arm core (running at 160 MHz) paired with 1640 KB of ROM memory for program storage and boot ROM, 544 KB of system-data RAM, and 1664 KB of code RAM. It also has 256 bytes of user-accessible OTP for storing wafer ID, RF/analog calibration settings, and other system configuration settings.

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2.DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

2.1.Absolute Maximum Ratings

Caution: The absolute maximum ratings in Table 1 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 1. Absolute maximum ratings

Rating	Symbol	Value	Unit
DC supply voltage for digital logic	VDDC	–0.5 to 0.828	V
DC supply voltage for baseband PLLs	BT_VDD_MISCLDO, VDDOUT_MISCLDO	–0.5 to 0.9844	V
DC supply voltage for RF analog	BT_LDO_VDD1P05, XTAL_VDD1P05	–0.5 to 1.2075	V
DC supply voltage for MISCLDO	LDO_VDD1P05	–0.5 to 1.2075	V
DC supply voltage for analog I/O	BT_VDD1P8, OTP_VDD1P8, PMU_VDD1P8	–0.5 to 2.07	V
DC supply voltage for Bluetooth PA	BT_VDD3P3_CORE0, BT_VDD3P3_CORE1	–0.5 to 3.795	V
DC supply voltage for digital I/O	PMU_VDDIO, VDDIO (VDDO pin)	–0.5 to 3.795	V
External TSSI input	TSSI	–0.5 to 1.5	V
Maximum undershoot voltage for I/O[a]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[a]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	110	°C

a. Duration not to exceed 25% of the duty cycle.

2.2.Environmental Ratings

The environmental ratings are shown in Table 2.

Table 2. Environmental ratings

Characteristic	Value	Unit	Conditions/Comments
Ambient Temperature (T_A)[a]	–40 to +85 (industrial part)	°C	Functional operation[b]
Storage Temperature	–40 to +125	°C	—
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

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a. See Table 26. Ordering information.

b. Functionality is guaranteed across this temperature range. Optimal RF performance specified in the data sheet, however, is guaranteed only for –10°C to +55°C without derating performance.

2.3.Recommended Operating Conditions and DC Characteristics

Caution: Functional operation is not guaranteed outside of the limits shown in Table 3, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 3. Recommended operating conditions and DC characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for digital logic	VDDC	0.6912	0.72	0.7488	V
DC supply voltage for baseband PLLs	BT_VDD_MISCLDO, VDDOUT_MISCLDO	0.8218	0.856	0.89	V
DC supply voltage for RF analog	BT_LDO_VDD1P05, XTAL_VDD1P05	1.008	1.05	1.092	V
DC input supply voltage for MISCLDO	LDO_VDD1P05	1.008	1.05	1.092	V
DC supply voltage for analog I/O	BT_VDD1P8, OTP_VDD1P8, PMU_VDD1P8	1.71	1.8	1.89	V
DC supply voltage for Bluetooth PA	BT_VDD3P3_CORE0, BT_VDD3P3_CORE1	3.135	3.3	3.465	V
DC supply voltage for digital I/O	PMU_VDDIO, VDDIO (VDDO pin)	3.135	3.3	3.465	V
External TSSI input	TSSI	0.30	—	1.1	V
Internal POR threshold	Vth_POR	0.4	—	0.7	V
Digital I/O Pins					
For 3.3V supply:					
Input high voltage	VIH	0.65 × VDDIO	—	—	V
Input low voltage	VIL	—	—	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.40	—	—	V
Output low voltage @ 2 mA	VOL	—	—	0.40	V

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2.4.Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 4. ESD specifications[a]

Condition	ESD Rating
Human body model (HBM) contact discharge	≥ 1.5 kV (margin capability) 1.0 kV (minimum capability)
Charged device model (CDM) contact discharge	≥ 350V (margin capability) 250V (minimum capability)

a. ESD specifications only apply to production parts. Applicable test specifications: ANSI/ESDA S20.20 2014 JS-001-2014 and
ANSI/ESDA S20.20 2014 JS-002-2014.

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3.Power Supplies and Power Management

3.1.Power Supply Topology

The SYN20708 contains a power management unit (PMU) and several LDO regulators. All regulators are programmable via the PMU. The PMU is powered by external 3.3V, 1.8V, and 1.05V supplies. All other voltages are provided by internal SYN20708 LDO regulators.

Figure 2 shows the typical SYN20708 power topology. The gray areas are external to the SYN20708.

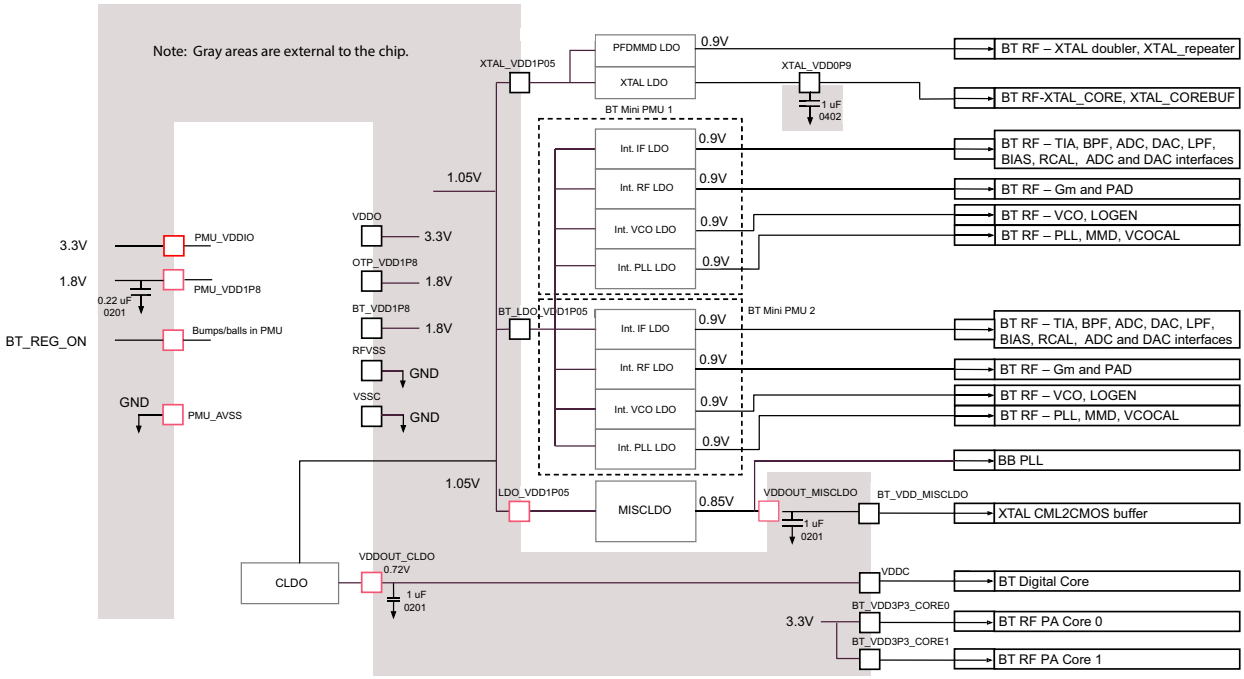

Figure 2. Typical power topology

3.2.Power Sequence

The SYN20708 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the SYN20708 is not needed in the system, VDDC is shut down via BT_REG_ON while VDDIO remains powered. This allows the SYN20708 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the SYN20708, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system.

When the SYN20708 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

Figure 3 shows the power sequence diagram.

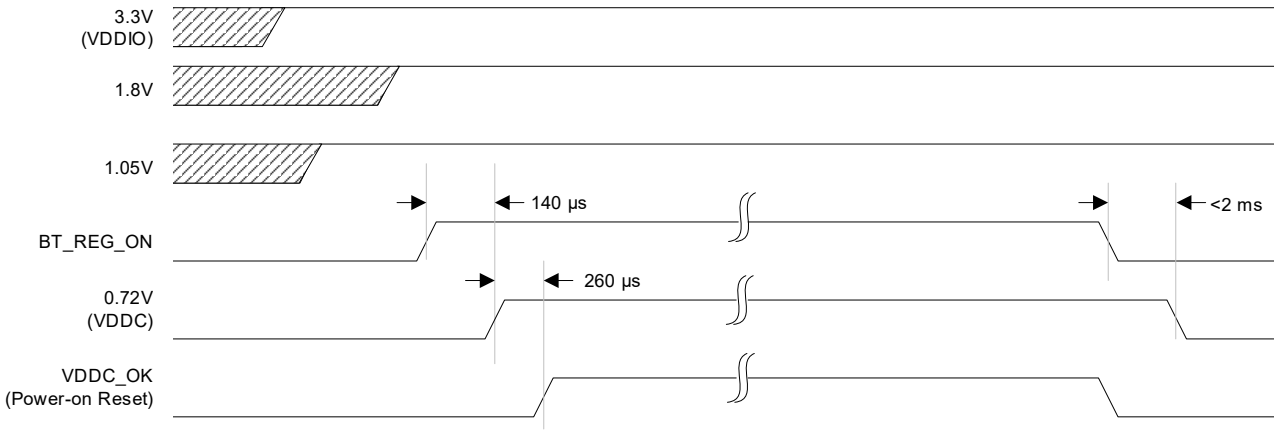

Figure 3. Power sequence diagram

3.3.Power and Reset Control

Table 5 provides the BT_REG_ON electrical specification.

Table 5. BT_REG_ON electrical specification

Parameter	Symbol	Conditions	Min.	Typical	Max.	Unit
Input high voltage	V_{IH}	For BT_REG_ON	1.08	—	3.465	V
Input low voltage	V_{IL}	—	VSS	—	0.3	V
Pull-down resistance	R_{PD}	—	—	100	—	kΩ
REG OFF time	T_{REG_OFF}	$C_{REG\_ON} \leq 10$ pF	—	—	2	ms

3.4.Power Management Unit Electrical Specification

Table 6 provides the PMU electrical specification.

Table 6. PMU electrical specification

Parameter	Pin Name	Conditions	Min.	Typical	Max.	Unit
I/O supply voltage 1	PMU_VDD1P8	—	1.71	1.80	1.89	V
I/O supply voltage 2	PMU_VDDIO	—	3.135	3.3	3.465	V
I/O supply voltage 3	LDO_VDD1P05	—	1.008	1.05	1.092	V
Power-up time	T_{PU}	CLDO output reaching 0.72V with respect to BT_REG_ON	—	171	—	µs
PMU_VDD1P8 and PMU_VDDIO power-down time	—	From 3.3V to 0.3V	—	—	10	ms

Table 7 provides the electrical specification of the internal regulators.

Table 7. Internal regulators electrical specification

Regulator	**Input Supply Voltage (V)**			**Output Current (mA)**			Nominal Output Voltage (V)
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
CLDO	0.9312	1.02	1.15	0.1	—	60	0.72
MISCLDO	0.9312	1.02	1.15	0.1	—	60	0.856

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4.Frequency References

An external crystal is used for generating all radio frequencies and normal-operation clocking.

4.1.Crystal Interface and Clock Generation

The SYN20708 uses an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

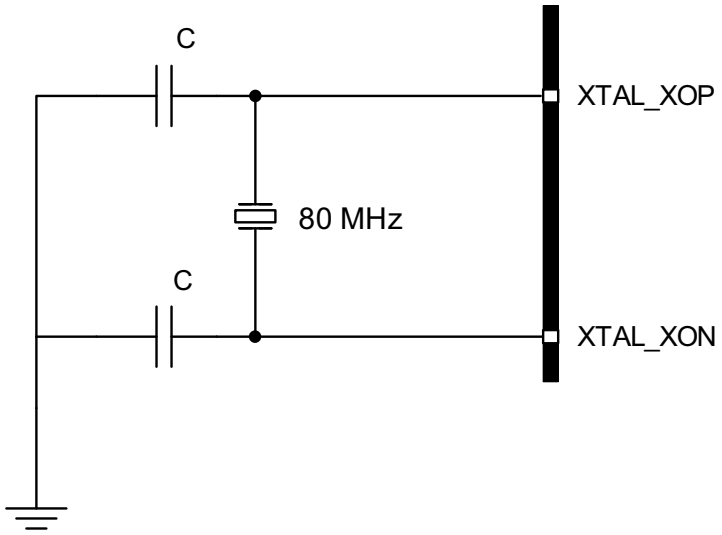


Figure 4. Recommended oscillator configuration

The recommended default frequency reference is an 80 MHz crystal. The signal characteristics for the crystal oscillator interface are provided in Table 8.

Note: Although the synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Synaptics for further details.

Table 8. Crystal oscillator requirements[a]

Parameter	Conditions/Notes	Crystal[b]			
		Min.	Typical	Max.	Unit
Frequency	—	—	80	—	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[c]	Without trimming	–20	—	20	ppm
Crystal load capacitance	—	—	8	—	pF
ESR	—	—	—	50	Ω

Table 8. Crystal oscillator requirements[a] (continued)

Parameter	Conditions/Notes	Crystal[b]			
		Min.	Typical	Max.	Unit
Drive level	External crystal must be able to tolerate this drive level.	150	—	—	µW

a. The parameter values in this table apply when using an 80 MHz crystal.

b. Use XTAL_XOP and XTAL_XON.

c. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

5.Bluetooth System Interfaces

5.1.UART Host Interface

The SYN20708 UART host interface is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 12 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 2600-byte receive FIFO and a 2600-byte transmit FIFO to support host-transport traffic. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.4 UART HCI specification: H4, a custom Extended H4, and H5, as well as the OpenThread Spinel protocol. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (*Three-wire UART Transport Layer*). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The SYN20708 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The SYN20708 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 9. Example of common Baud rates

Desired Rate	Actual Rate	Error (%)
12000000	12000000	0.00
9600000	9600000	0.00
8000000	8000000	0.00
6000000	6000000	0.00
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

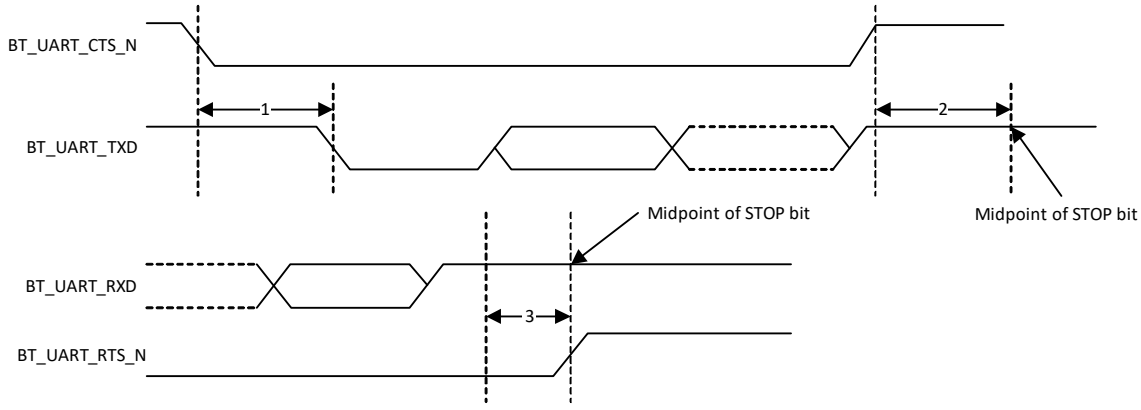


Figure 5. UART timing

Table 10. UART Timing specifications

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods

5.2.Peripheral/Debug UART Interface

The peripheral/debug UART has the following features:

- 256-byte RX and TX FIFOs.
- A 4-pin interface.

The PUART_RXD and PUART_TXD signals can be multiplexed to one of the following three pairs of pins, respectively:

- ETRSW_CTRL0 and ETRSW_CTRL1
- ANT_SEL2 and ANT_SEL1
- TX_CONFX2 and BT_STATUS2

Table 11 shows the rates supported by the peripheral/debug UART.

Table 11. Peripheral/Debug UART supported rates

Desired Rate	Actual Rate	Error (%)
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

5.3.Serial Flash Interface

The serial flash interface supports the following features:

- A SPI-compatible serial bus.
- A maximum serial flash size of 64 MB.
- A 24 MHz (maximum) clock frequency.
- Support for either ×1 or ×4 addresses with two data lines (one input and one output).
- 3-byte and 4-byte addressing modes.
- A configurable dummy-cycle count that is programmable from 1 to 15.
- Programmable instructions output to serial flash.
- An option to change the sampling edge from rising-edge to falling-edge for read-back data when in high-speed mode.

Note: To minimize ripple at the SYN20708 SPI_CLK port to within ±20% of VDDIO due to transmission-line effects, use a series resistor on the SPI_CLK line to the serial flash, preferably close to the serial flash port.

5.3.1.Serial Flash Timing

5.3.1.1.Read-Register Timing

Figure 6 shows the serial flash extended read–register timing.

Note: Regarding Figure 6, all Read Register commands except Read Lock Register are supported. A Read Nonvolatile Configuration Register operation will output data starting from the least significant byte.

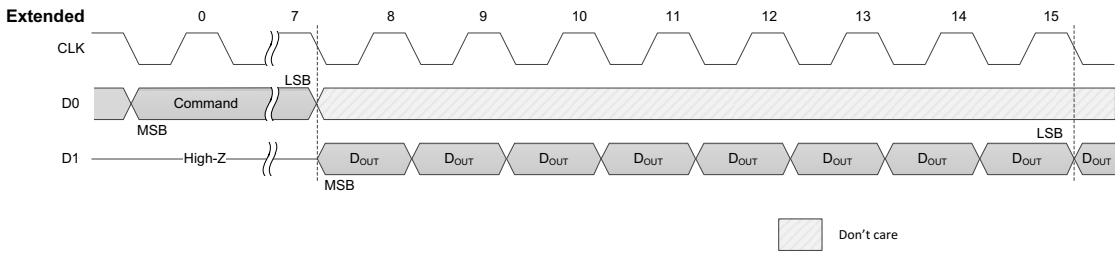


Figure 6. Serial flash read-register timing

5.3.1.2.Write-Register Timing

Figure 7 shows the serial flash extended write–register timing.

Note: Regarding Figure 7:

- All write-register commands except Write Lock Register are supported.
- The waveform must be extended for each protocol to 23.
- A Write Nonvolatile Configuration Register operation requires data to be sent starting from the least significant byte.

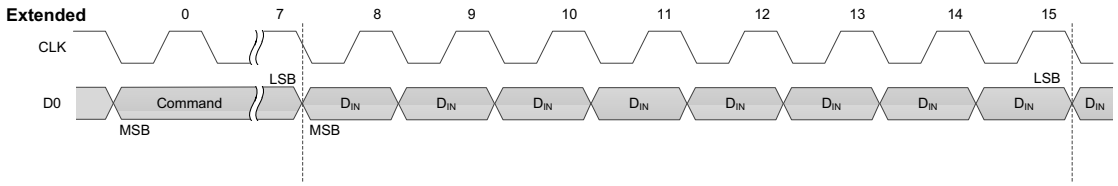


Figure 7. Serial flash write-register timing

5.3.1.3.Memory Fast-Read Timing

Figure 8 shows the serial flash extended memory fast-read timing.

Note: Regarding Figure 8:

- 24-bit addressing is used, so A[MAX] = A[23] and A[MIN] = A[0].
- For an extended SPI protocol, C_X = 7 + (A[MAX] + 1).

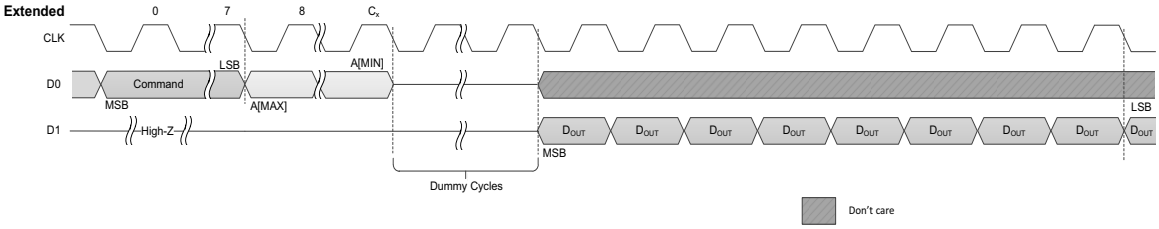


Figure 8. Memory fast-read timing

5.3.1.4.Memory-Write Timing

Figure 9 shows the serial flash extended memory-write (Page Program) timing.

Note: Regarding Figure 9, for an extended SPI protocol, C_X = 7 + (A[MAX] + 1).

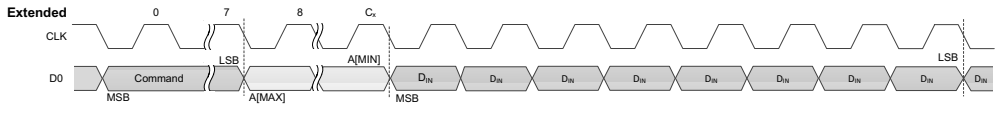


Figure 9. Memory-write timing

5.3.2.Serial Flash Parameters

The combination of Figure 10 and Table 12 provides the serial flash timing parameters.

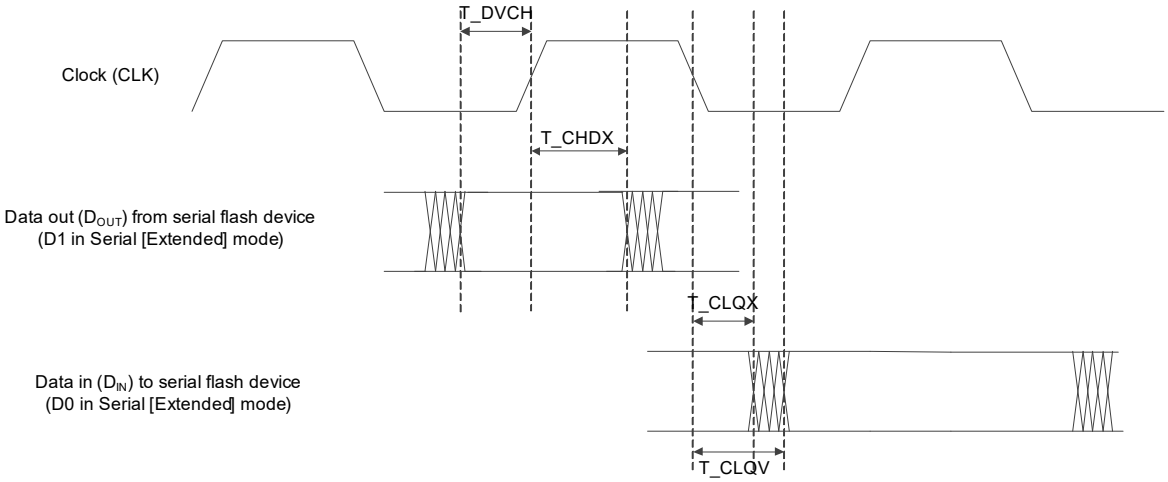


Figure 10. Serial flash timing parameters diagram

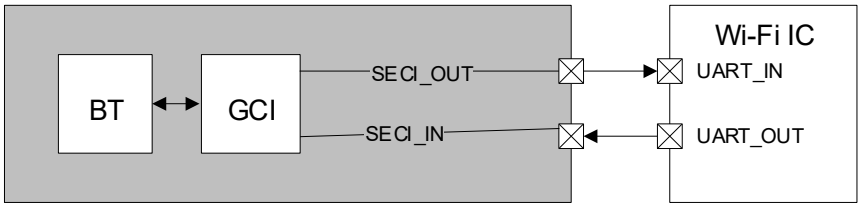
Table 12. Serial flash timing parameters

Parameter	Description	Minimum	Maximum	Unit
T_DVCH	Data setup time	2	–	ns
T_CHDX	Data hold time	3	–	ns
T_CLQX	Output hold time	1	–	ns
T_CLQV	Output valid time (with a 10 pF load)	–	5	ns

5.3.3.Serial Enhanced Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as a Wi-Fi IC, to manage wireless medium sharing for optimum performance.

Figure 11 shows the Wi-Fi coexistence interface. See Table 10, “UART Timing specifications,” on page 17 for UART baud rate.



NOTE: SECI_OUT and SECI_IN are multiplexed on the GPIOs.

Figure 11. Serial enhanced coexistence interface

5.4.I²C Interface

The SYN20708 supports a I²C master interface. The Standard, Fast, and Fast-mode Plus modes are supported.

The I²C interface is a 2-wire serial bus that is compatible with the I²C Specification (version 2.1). The SYN20708 I²C interface supports the following features:

- Parallel-to-I²C bus protocol converter and interface.
- Standard mode (100 kbps), Fast mode (400 kbps), and Fast-mode Plus (1 Mbps).
- Single-master capability.
- Support for both 7-bit and 10-bit addressing.
- Available as a GPIO alternate function.
- Clock and data glitch filtering.

The SCL and SDA signals can be multiplexed to one of the following four pairs of pins, respectively:

- TDO and TDI.
- EPA_CTRL1 and EPA_CTRL0.
- ANT_SEL1 and ANT_SEL2.
- SPI_MISO and SPI_MOSI.

The I²C interface timing specifications are defined in Table 13 and Figure 12.

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Table 13. I²C timing specifications

Parameter	Symbol	Fast-mode Plus[a,b]			Unit
		Minimum	Typical	Maximum	
SCL clock frequency	f_{SCL}	0	—	1000	kHz
Bus-free times between a stop and start condition	t_{Buf}	500	—	—	ns
Hold time (repeated) start condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	260	—	—	ns
Low period of the SCL clock	t_{LOW}	500	—	—	ns
High period of the SCL clock	t_{HIGH}	260	—	—	ns
Set-up time for a repeated start condition	$t_{SU;STA}$	260	—	—	ns
Data hold time	$t_{HD;DAT}$	0[c]	—	450[d]	ns
Data setup time	$t_{SU;DAT}$	260[e]	—	—	ns
Setup time for stop condition	$t_{SU;STO}$	260	—	—	ns
Pulse width of spikes suppressed by the input filter	t_{SP}	0	—	10	ns

a. All timing values are referenced to minimum (V_{IH}) and maximum (V_{IL}) levels and were obtained over process, voltage, and temperature.

b. For Fast-mode Plus, the hardware currently supports the 4th mode, not the 3rd mode.

c. A device must internally provide a hold time of at least 300 ns for the serial data (SDA) signal to bridge the undefined region of the serial clock line (SCL).

d. This must be met because the SYN20708 does not stretch the low period of the SCL signal.

e. A Fast-mode Plus device can be used in Fast mode or Standard mode, but the $T_{SU,DAT}$ > 100 ns (Fast mode) or $T_{SU;DAT}$ > 250 ns (Standard mode) requirement must be met. This automatically applies because the SYN20708 does not stretch the low period of the SCL signal for Fast-mode Plus.

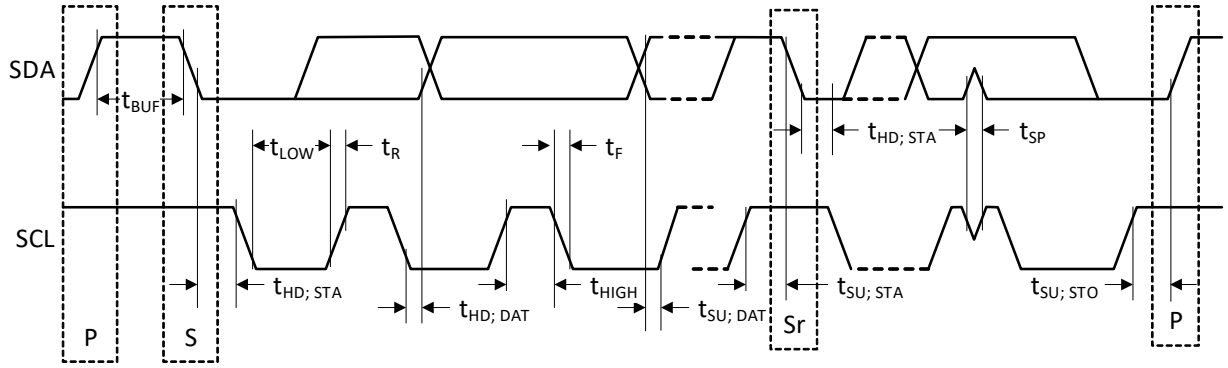

Figure 12. Clock and data timing

The SDA and SCL lines can source and sink 2 mA and have internal 45 kΩ pull-up resistors. To drive the capacitive load of the I²C interface, external pull-up resistors will be required to keep the rise time less than 300 ns between 30% of VDD_IO and 70% of VDD_IO. The rise time is modeled by a

simple RC circuit where R is the total pull-up resistance (the parallel combination of the internal and external resistors) and C is the total capacitance of the signal line, the trace capacitance, and all connected pins.

$V(t) = VDD\_IO \times (1 - e^{-t/RC})$

Since the rise time from 30% to 70% of VDD_IO must be less than 300 ns, the maximum value of R is:

$R_{max} < (300 \times 10^{-9})/(0.8473 \times C)$

The minimum value of R is limited by the 2 mA pull-down capability of the SDA and SCL drivers:

$R_{min} > (VDD\_IO / 2\ mA)$

This gives minimum R values of 900Ω when VDD_IO is 1.8V. Taking into consideration the minimum value of the internal 35 kΩ pull-up (R_{int}), the value of the external resistor (R_{ext}) is:

$R_{ext} = (R \times R_{int})/(R_{int} - R)$

Thus, if the calculated total pull-up value of R is 900Ω, then the minimum value of R_{ext} is 924Ω for a line with very high capacitance. A value of 1.8 kΩ for R_{ext} is usually sufficient.

5.5.Antenna Selection Interface

The SYN20708 supports up to four pins (ANT_SEL0–ANT_SEL3) that can be used to connect to a 16-antenna array for AoA, AoD, or channel sounding (CS). (CS uses a maximum of four antennas.) These pins are programmed as outputs when they are used to control an external RF switch, and they are designed to support switching speeds as fast as one µs.

Table 14 describes the four pins when they're used as antenna-switching control signals.

Table 14. Antenna switching control pins

Pin Name	Description
ANT_SEL0	Defaults as bit 0 of an AoA, AoD, or CS antenna selection.
ANT_SEL1	Defaults as bit 1 of an AoA, AoD, or CS antenna selection.
ANT_SEL2	Defaults as bit 2 of an AoA or AoD antenna selection.
ANT_SEL3	Defaults as bit 3 of an AoA or AoD antenna selection.

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6.Bluetooth and IEEE 802.15.4 RF Specifications

6.1.Introduction

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 2, "Environmental ratings," on page 7 and "Recommended Operating Conditions and DC Characteristics" on page 8.

Typical values apply for an ambient temperature of +25°C.

Figure 13 shows the Bluetooth RF port configuration. Separate RX and TX can be accommodated for external PAs and LNAs.

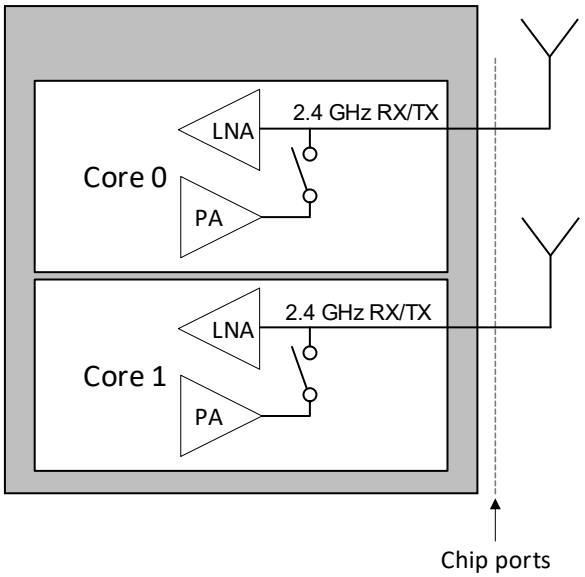

Figure 13. Bluetooth RF port configuration

Note: Unless otherwise specified, all Bluetooth specifications are measured at the chip port.

6.2.Bluetooth 2.4 GHz Receiver Performance Specification

Note: Table 15 applies to each radio, and unless otherwise defined, all values are measured at the chip RF input port.

Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions		Min	Typical	Max	Unit
General						
Frequency Range		—	2402	—	2480	MHz

Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions			Min	Typical	Max	Unit
Receive sensitivity with dirty transmit off (BDR and EDR modes)	Normal-Power mode, no MRC	1 Mbps, GFSK BDR, 0.1% BER		—	-92.5	-90	
		2 Mbps, π/4-DQPSK EDR-2, 0.01% BER		—	-95	-92	
		3 Mbps, 8-DQPSK EDR-3, 0.01% BER		—	-89	-86	
	Normal-Power mode with MRC	1 Mbps, GFSK BDR, 0.1% BER		—	-95	—	
		2 Mbps, π/4-DQPSK EDR-2, 0.01% BER		—	-98	—	
		3 Mbps, 8-DQPSK EDR-3, 0.01% BER		—	-92	—	
Receive sensitivity with dirty transmit off (BLE modes)	Normal-Power mode, no MRC	37-byte payload, standard modulation index, 30.8% PER	125 kbps	—	– 108.5	–106	dBm
			500 kbps	—	– 103.5	–101	dBm
			1 Mbps	—	– 97.5	–95	dBm
			2 Mbps	—	– 94.5	–92	dBm
		255-byte payload, standard modulation index, 30.2% PER	125 kbps	—	– 108.5	–106	dBm
			500 kbps	—	– 102.5	–100	dBm
			1 Mbps	—	– 96.5	–94	dBm
			2 Mbps	—	– 93.5	–91	dBm
	Normal-Power mode with MRC	37-byte payload, standard modulation index, 30.8% PER	125 kbps	—	– 111.5	—	dBm
			500 kbps	—	– 106.5	—	dBm
			1 Mbps	—	– 100.5	—	dBm
			2 Mbps	—	– 97.5	—	dBm
		255-byte payload, standard modulation index, 30.2% PER	125 kbps	—	– 111.5	—	dBm
			500 kbps	—	– 105.5	—	dBm
			1 Mbps	—	– 99.5	—	dBm
			2 Mbps	—	– 96.5	—	dBm

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Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions	Min	Typical	Max	Unit
Receive sensitivity degradation on spurious	BDR, EDR-2, EDR-3 BLE (125 kbps, 500 kbps, 1 Mbps, and 2 Mbps)	—	—	2	dB
Input in-band IIP3	Maximum LNA gain	−12	—	—	dBm
	Minimum LNA gain	0	—	—	dBm
Maximum receive	BDR, EDR-2, EDR-3	-17	—	—	
	BLE (125 kbps, 500 kbps, 1 Mbps, and 2 Mbps)	-10	—	—	dBm
No damage max.	BDR, EDR-2, EDR-3, BLE modes	13	—	—	dBm
RX LO leakage	BDR, EDR-2, EDR-3, BLE modes	—	—	−50	dBm/ MHz
RSSI accuracy with calibration @ system level. See section 12.4.3 of the requirements	Connected modes	−2	—	2	dBm
	BLE scan mode (when listening to BLE advertisement channels)	−2	—	2	dBm
	BLE connected mode	−2	—	2	dBm
General spurs (LO, AFE, VCO, XTAL+LO),	—	—	—	−50	dBm/ MHz
Return loss	Z_0 = 50Ω across the RX dynamic range	—	10	—	dB
Interference Performance [a]					
C/I co-	GFSK, 0.1% BER	—	—	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	—	—	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	—	—	−30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	—	—	−40	dB
C/I image channel	GFSK, 0.1% BER	—	—	−9	dB

Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions	Min	Typical	Max	Unit
C/I 1 MHz adjacent to image	GFSK, 0.1% BER	—	—	–20	dB
C/I co-	π/4-DQPSK, 0.1% BER	—	—	13	dB
C/I 1 MHz	π/4-DQPSK, 0.1% BER	—	—	0	dB
C/I 2 MHz	π/4-DQPSK, 0.1% BER	—	—	–30	dB
C/I ≥ 3 MHz	π/4-DQPSK, 0.1% BER	—	—	–40	dB
C/I image	π/4-DQPSK, 0.1% BER	—	—	–7	dB
C/I 1 MHz	π/4-DQPSK, 0.1% BER	—	—	–20	dB
C/I co-	8-DPSK, 0.1% BER	—	—	21	dB
C/I 1 MHz	8-DPSK, 0.1% BER	—	—	5	dB
C/I 2 MHz	8-DPSK, 0.1% BER	—	—	–25	dB
C/I ≥ 3 MHz	8-DPSK, 0.1% BER	—	—	–33	dB
C/I image	8-DPSK, 0.1% BER	—	—	0	dB
C/I 1 MHz	8-DPSK, 0.1% BER	—	—	–13	dB
Out-of-Band Blocking Performance (CW)					
Normal-Power mode	30–2000 MHz 0.1% BER	—	–10	—	dBm
	2000–2399 MHz 0.1% BER	—	–27	—	dBm
	2498–3000 MHz 0.1% BER	—	–27	—	dBm
	3000 MHz–12.75 GHz 0.1% BER	—	–27	—	dBm
Out-of-Band Blocking Performance, Modulated Interferer [b] [c]					

Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions		Min	Typical	Max	Unit
Normal-Power mode Applies to GFSK (1 Mbps), π/4-DPSK (2 Mbps), and 8-DPSK (3 Mbps)	600–960 MHz	LB1 with LTE and WCDMA signal	–25	–15	—	dBm
	1700–2025 MHz	MB with LTE and WCDMA signal	–25	–15	—	dBm
	824–849 MHz	GSM850 with GSM signal	–23	–15	—	dBm
	880–915 MHz	E-GSM with GSM signal	–23	–15	—	dBm
	1710–1785 MHz	GSM1800 with GSM signal	–25	–15	—	dBm
	1850–1910 MHz	GSM1800 with GSM signal	–25	–25	—	dBm
	2300–2370 MHz	B40A with LTE signal	—	–25	—	dBm
	2330–2370 MHz	B40B with LTE signal	—	TBD[d]	—	dBm
	2370–2400 MHz	B40B with LTE signal	—	–35	—	dBm
	2400–2483.5 MHz	ISM with WLAN reference signal	–46	TBD	—	dBm
	2496–2510 MHz	B41 with LTE signal	—	–25	—	dBm
	2510–2690 MHz	B41 with LTE signal	—	–15	—	dBm
	3400–3800 MHz	B42/43 w/LTE signal	–25	–15	—	dBm
	3300–4200 MHz	5G NR n77	–25	–15	—	dBm
	4400–5000 MHz	5G NR n79	–25	–15	—	dBm
	5150–5925 MHz	WLAN HT20 MCS0 signal	–30	–15	—	dBm
	6240–7987 MHz	UWB CH5–CH8 signal	–30	–15	—	dBm
	7488–8736 MHz	UWB CH9–CH10 signal	–30	–15	—	dBm
Spurious Emissions						

Table 15. Bluetooth 2.4 GHz receiver specification (derived from simulation)

Parameter	Conditions	Min	Typical	Max	Unit
Normal-Power mode	30 MHz–1 GHz	—	-90	—	dBm
	1–12.75 GHz	—	-90	—	dBm
	851–894 MHz	—	-165	—	dBm/ Hz
	925–960 MHz	—	-165	—	dBm/ Hz
	1805–1880 MHz	—	-165	—	dBm/ Hz
	1930–1990 MHz	—	-165	—	dBm/ Hz
	2110–2170 MHz	—	-165	—	dBm/ Hz

a. The maximum value represents the actual Bluetooth Low Energy specification required for Bluetooth Low Energy qualification as defined in the version 4.7 specification.
b. For LTE bands, measure 3 dB RX sensitivity degradation with 16-QAM 1 RB, 12 RB, 25 RB, and 100 RB uplink signals. Use 200 RB where applicable. For 2.4 GHz ISM band, measure 3 dB RX sensitivity degradation with a WLAN HT20 MCS0 jammer signal. The WLAN jammer is set for 2437 MHz; the desired Bluetooth signal is offset ±30 MHz (typical), ±15 MHz (minimum).
c. Blocking level for 3 dB RX sensitivity degradation at the chip input for the modulation indicated with a 0.01% BER and without external filtering.
d. Due to a notch filter limitation, this can't be measured accurately.

6.3. Bluetooth 2.4 GHz Transmitter Performance Specification

Note: Table 16 applies to each core, and unless otherwise defined, all values are measured at the chip RF input port.

Table 16. Bluetooth 2.4 GHz transmitter RF specification (derived from simulation)

Parameter	Conditions		Min.	Typical	Max.	Unit
General						
Frequency range		—	2402	—	2480	MHz

Table 16. Bluetooth 2.4 GHz transmitter RF specification (derived from simulation) (continued)

Parameter	Conditions		Min.	Typical	Max.	Unit
TX output power (TX power at chip output that meets *Bluetooth Test Specification RF.TS.4.0.0 ACP/EVM* requirements. Also, all TX output power requirements shall be met for 2:1 VSWR for all phase angles over VT.	Normal-Power mode	BDR, GFSK	—	14	—	—
		EDR-2, π/4-DQPSK	—	11	—	—
		EDR-3, 8-DPSK	—	11	—	—
		BLE (1 Mbps, 2 Mbps, 500 kbps, and 125 kbps), GFSK	—	14	—	dBm
	Beamforming mode	BDR, GFSK	—	20	—	—
		EDR-2, π/4-DQPSK	—	15	—	—
		EDR-3, 8-DPSK	—	15	—	—
		BLE (1 Mbps, 2 Mbps, 500 kbps, and 125 kbps), GFSK	—	20	—	dBm
	High-Power mode (with ePA)	BLE (1 Mbps, 2 Mbps, 500 kbps, and 125 kbps), GFSK	Dependent on the external PA and board design.			dBm
Output power variation with 3:1 VSWR (Chip shall meet all ACP/EVM requirements specified in *Bluetooth Test Specification RF.TS.4.0.0* under 3:1 VSWR for all phase angles.)	—		–2	—	2	dB
Power control step	—		2	4	8	dB
Power control accuracy over process (Output power will include calibration.)	BDR, EDR-2, EDR-3,BLE modes		–1	—	1	dB
TX power control dynamic range	Applies to both the BT normal-power and high-power modes		—	30	—	dB
Gain control step	For setting output power		—	—	0.25	dB
Return loss at chip TX port	Z_0 = 50Ω, across the TX dynamic range		—	8	—	dB
BDR GFSK TX output spectrum	-20 dBc BW (20 dB bandwidth)		—	0.93	1	—

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Table 16. Bluetooth 2.4 GHz transmitter RF specification (derived from simulation) (continued)

Parameter		Conditions	Min.	Typical	Max.	Unit
In-Band Spurious Emissions [a]						
EDR	1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency	—	–38	–26	—
	1.5 MHz < |M – N| < 2.5 MHz		—	–30	–20	—
	|M – N| ≥ 2.5 MHz		—	–43	–40	—
BLE	1.5 MHz < |M – N| < 2.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	—	–45	–20	dBm
	|M – N| ≥ 2.5 MHz [b]		—	–50	–30	dBm
BLE2	3.5 MHz < |M – N| < 4.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	—	–50	–20	dBm
	4.5 MHz < |M – N| < 5.5 MHz		—	–50	–20	dBm
	|M – N| ≥ 5.5 MHz		—	–55	–30	dBm

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Table 16. Bluetooth 2.4 GHz transmitter RF specification (derived from simulation) (continued)

Parameter	Conditions		Min.	Typical	Max.	Unit
Out-of-Band Emissions [a]						
TX harmonics (HD2, HD3, HD4) Chip Pout = 14 dBm, BDR and BLE modes	Normal-Power mode	HD2 with TX at full power	—	–15	—	dBm/MHz
		HD3 with TX at full power	—	–18	—	dBm/MHz
		HD4 with TX at full power	—	–30	—	dBm/MHz
	Beamforming mode	HD2 with TX at full power	—	–9	—	dBm/MHz
		HD3 with TX at full power	—	–14	—	dBm/MHz
		HD4 with TX at full power	—	–25	—	dBm/MHz
TX spurs Chip Pout = 14 dBm, BDR and BLE modes	Normal-Power mode	VCO spur at fundamental frequency over the full TX dynamic range	—	–50	—	dBm/MHz
		30 MHz to 1 GHz	—	–47	—	dBm/MHz
		1 GHz to 12.75 GHz	—	–35	—	dBm/MHz
		1.8 GHz to 1.9 GHz	—	N/A[c]	—	dBm/MHz
		5.15 GHz to 5.3 GHz	—	N/A[c]	—	dBm/MHz
	Beamforming mode	VCO spur at fundamental frequency over the full TX dynamic range	—	–45	—	dBm/MHz
		30 MHz to 1 GHz	—	–43	—	dBm/MHz
		1 GHz to 12.75 GHz	—	–29	—	dBm/MHz
		1.8 GHz to 1.9 GHz	—	N/A	—	dBm/MHz
		5.15 GHz to 5.3 GHz	—	N/A	—	dBm/MHz

Table 16. Bluetooth 2.4 GHz transmitter RF specification (derived from simulation) (continued)

Parameter	Conditions		Min.	Typical	Max.	Unit
Noise floor	Normal-Power mode	600–960 MHz	—	–163	—	dBm/Hz
		1170–1184 MHz (GPS L5)	—	–158	—	dBm/Hz
		1570–1610 MHz (GPS + GLONASS)	—	–153	—	dBm/Hz
		1440–1520 MHz (B11, B21, B32)	—	–154	—	dBm/Hz
		1805–1880 MHz (GSM + WCDMA)	—	–148	—	dBm/Hz
		1900–1920 MHz (GSM + WCDMA)	—	–148	—	dBm/Hz
		1930–1990 MHz (GSM + WCDMA)	—	–147	—	dBm/Hz
		2010–2025 MHz (TDSCDMA)	—	–146	—	dBm/Hz
		2110–2170 MHz (WCDMA)	—	–143	—	dBm/Hz
		2300–2370 MHz (B40 TDD)	—	–128	—	dBm/Hz
		2510–2690 MHz	—	–128	—	dBm/Hz
		3400–3800 MHz (B42, B43)	—	–148	—	dBm/Hz
		3800–4200 MHz (5G NR n77)	—	–148	—	dBm/Hz
		4400–5000 MHz (5G NR n79)	—	–148	—	dBm/Hz
		5150–5925 MHz	—	–156	—	dBm/Hz
		5925–6525 MHz (UNII-5–6, UWB CH5)	—	–160	—	dBm/Hz
		7737–8237 MHz (UWB CH9)	—	–160	—	dBm/Hz

a. **Applicable to BT normal-power mode TX.**
b. The typical number is measured at ±3 MHz offset.
c. No visible spurs above the noise floor.

6.4.Bluetooth Local Oscillator Performance

Table 17. Local oscillator performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	—	72	—	µs
Initial carrier frequency tolerance	—	±25	±75	kHz
Frequency Drift				
DH1 packet	—	±8	±25	kHz
DH3 packet	—	±8	±40	kHz
DH5 packet	—	±8	±40	kHz
Drift rate	—	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	—	kHz
Channel spacing	—	1	—	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

6.5.IEEE 802.15.4 Receiver and Transmitter RF Performance

Table 18. IEEE 802.15.4 receiver and transmitter RF specification

Parameter	Conditions	Min.	Typical	Max.	Unit
Frequency range	—	2402	—	2480	MHz
Receiver Specification					
Receive sensitivity with dirty transmit off	250 kbps, OQPSK, 1% PER	—	–106	–103.5	dBm
Adjacent channel interference	1% PER	0	—	—	dB
Alternate adjacent channel interference	1% PER	30	—	—	dB
Transmitter Specification					

Table 18. IEEE 802.15.4 receiver and transmitter RF specification (continued)

Parameter	Conditions	Min.	Typical	Max.	Unit
TX output power at the chip output that meets the IEEE 802.15.4 EVM requirement.	OQPSK. 2:1 VSWR for all phase angles over voltage and temperature.	13	—	—	dBm
TX output spectrum mask	$\|f - f_c\| > 3.5$ MHz (relative)	—	—	−25	dBc
	$\|f - f_c\| > 3.5$ MHz (absolute)	—	—	−35	dBm

7.Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Unless otherwise stated, these values apply for the conditions specified in Table 3. The BLE power consumption measurements are shown in Table 19.

Table 19. Bluetooth and BLE power consumption[a]

	Operating Mode	VDDrail = 3.3V (mW)	VDDrail = 1.05V (mW)	VDDrail = 1.8V (mW)
Idle mode		TBD	TBD	TBD
Receive Modes				
Normal mode	BDR	2.48	27.72	0.30
Normal mode	EDR	2.48	28.04	0.30
Normal mode	BLE	2.72	26.88	0.30
Concurrent mode maximal ratio combining (MRC)	BDR	2.64	35.91	0.32
Concurrent mode maximal ratio combining (MRC)	EDR	2.67	36.44	0.32
Concurrent mode maximal ratio combining (MRC)	BLE	2.63	33.92	0.32
Transmit Modes				
Normal mode	BDR(14 dBm output power per core)	135.83	47.15	0.30
Normal mode	EDR(11 dBm output power per core)	104.18	42.41	0.30
Normal mode	BLE (14 dBm output power per core)	116.03	46.66	0.30
Concurrent mode beamforming	BDR (20 dBm output power, combined)	227.70	62.27	0.32
Concurrent mode beamforming	EDR (17 dBm output power, combined)	190.08	56.18	0.32
Concurrent mode beamforming	BLE (20 dBm output power, combined)	229.94	65.30	0.32

a. The power consumption is estimated assuming typical operating conditions at 25°C.

8.Package Information

8.1.Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	ANT_SEL0	ANT_SEL2		EPA_CTRL1			SECI_IN			TCK		ETRSW_CTRL0	ETRSW_CTRL1	A
B	ANT_SEL3	ANT_SEL1	RF_ACTIVE2	BT_GPIO_2		JTAG_CE	SECI_OUT		TMS	TRST	TDO	TDI	BT_ANALOG_IO_CORE1	B
C		SW_RESET_B	SPI_CLK	TX_CONFX2	BT_STATUS	VSSC	HW_RESET_B	SYS_RESET_B	VSSC	VSSC	VSSC	RFVSS	RFVSS	C
D			SPI_MISO	VSSC	VSSC							RFVSS	BT_TX_CORE1	D
E	SPI_CSB	SPI_MOSI	VSSC				VDDO				BT_VDD3P3_CORE1	RFVSS	RFVSS	E
F		UART_TXD	VSSC									RFVSS	BT_RF_CORE1	F
G		UART_RXD	VSSC		VSSC	VDDC			BT_LDO_VDD1P05			RFVSS	RFVSS	G
H	UART_CTS	UART_RTS	VSSC		VDDC	VSSC						RFVSS	BT_RF_CORE0	H
J	BT_STATUS2	TEST_ENABLE	VSSC								BT_VDD3P3_CORE0	RFVSS	RFVSS	J
K		EPA_CTRL0	PMU_AVSS	VDDOUT_CLDO								RFVSS	BT_TX_CORE0	K
L	MODE_SEL	VSSC	PMU_AVSS	VDDOUT_MISCLDO				BT_VDD_MISCLDO		RFVSS	RFVSS	RFVSS	RFVSS	L
M	PMU_AVSS	PMU_AVSS	PMU_AVSS	PMU_AVSS	PMU_AVSS	BT_REG_ON	BT_ANALOG_IO_CORE0	RFVSS	RFVSS	XTAL_XOP	XTAL_XON	RFVSS	BT_VDD1P8	M
N	PMU_AVSS	LDO_VDD1P05	PMU_AVSS	PMU_VDDIO	PMU_VDD1P8	OTP_VDD1P8		RFVSS	XTAL_VDD0P9			XTAL_VDD1P05	RFVSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 14. SYN20708 FCBGA pin map

8.2.Signal Descriptions

Table 20 provides the signal name, type, and description of each pin in the SYN20708. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 20. SYN20708 FCBGA signal descriptions

Signal Name	Pin (Bump)	Type	Description
RF Signal Interface			
BT_ANALOG_IO_CORE0	M7	I	Bluetooth core 0 external TSSI or analog input
BT_ANALOG_IO_CORE1	B13	I	Bluetooth core 1 external TSSI or analog input

Table 20. SYN20708 FCBGA signal descriptions (continued)

Signal Name	Pin (Bump)	Type	Description
BT_RF_CORE0	H13	I/O	Bluetooth core 0 radio receiver input and transmitter output
BT_RF_CORE1	F13	I/O	Bluetooth core 1 radio receiver input and transmitter output
BT_TX_CORE0	K13	O	Bluetooth core 0 radio transmitter output
BT_TX_CORE1	D13	O	Bluetooth core 1 radio transmitter output
Coexistence Interface			
SECI_IN	A7	I	SECI_IN when used with another Synaptics device; otherwise, TX confirmation (TX_CONFX) input of a primary 3-wire Bluetooth coexistence interface.
SECI_OUT	B7	O	SECI_OUT when used with another Synaptics device; otherwise, RF active (RF_ACTIVE) output of a primary 3-wire Bluetooth coexistence interface.
Crystal (XTAL) Interface			
XTAL_XON	M11	O	XTAL oscillator output
XTAL_XOP	M10	I	XTAL oscillator input
Grounds			
PMU_AVSS	K3, L3, M1, M2, M3, M4, M5, N1, N3	GND	Analog ground
RFVSS	C12, C13, D12, E12, E13, F12, G12, G13, H12, J12, J13, K12, L10, L11, L12, L13, M8, M9, M12, N8, N13	GND	RF ground
VSSC	C6, C9, C10, C11, D4, D5, E3, F3, G3, G5, H3, H6, J3, L2	GND	Core ground

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Table 20. SYN20708 FCBGA signal descriptions (continued)

Signal Name	Pin (Bump)	Type	Description
Miscellaneous Signals			
ANT_SEL0	A1	O	Defaults as bit 0 of an angle of arrival (AoA), angle of departure (AoD), or channel sounding (CS) antenna selection.
ANT_SEL1	B2	O	Defaults as bit 1 of an AoA, AoD, or CS antenna selection. Also usable as the PUART RTS_N signal.
ANT_SEL2	A2	I/O	Defaults as bit 2 of an AoA or AoD antenna selection. Also usable as the PUART CTS_N signal.
ANT_SEL3	B1	I/O	Defaults as bit 3 of an AoA or AoD antenna selection. Also usable as GPIO_3.
BT_GPIO_2	B4	I/O	GPIO_2. Usable as an external interrupt source.
BT_REG_ON	M6	I	0: Turn internal PMU off. 1: Turn internal PMU on.
BT_STATUS	C5	O	STATUS output line of a primary 3-wire Bluetooth coexistence interface
BT_STATUS2	J1	O	Usable as the PUART TXD signal. Also usable as the STATUS output line of a secondary 3-wire Bluetooth coexistence interface.
EPA_CTRL0	K2	I/O	Defaults as an external PA (ePA) control output for core 0. Also usable as the PUART RTS_N signal or GPIO_4.
EPA_CTRL1	A4	I/O	Defaults as an ePA control output for core 1. Also usable as the PUART CTS_N signal or GPIO_5.
ETRSW_CTRL0	A12	O	External TR switch control for core 0.
ETRSW_CTRL1	A13	O	External TR switch control for core 1.
HW_RESET_B	C7	I	External active-low hardware reset. Warm reset that triggers a FW download.
JTAG_CE	B6	I	JTAG chip-enable input

Table 20. SYN20708 FCBGA signal descriptions (continued)

Signal Name	Pin (Bump)	Type	Description
MODE_SEL	L1	I	Mode selection: 0: MCM mode 1: Standalone mode
RF_ACTIVE2	B3	O	RF_ACTIVE output line of a secondary 3-wire Bluetooth coexistence interface or usable as a debugging port
SW_RESET_B	C2	I	External active-low software reset. Warm reset that does not trigger a FW download.
SYS_RESET_B	C8	I	External active-low system reset
TCK	A10	I	TCK signal
TDI	B12	I	TDI signal
TDO	B11	O	TDO signal
TEST_ENABLE	J2	I	0: Normal operating mode 1: Test mode.
TMS	B9	I	TMS signal
TRST	B10	I	Test reset
TX_CONFX2	C4	I	Usable as the PUART RXD signal. Also usable as the TX confirmation (TX_CONFX) input of a secondary 3-wire Bluetooth coexistence interface.
Serial Peripheral Interface			
SPI_CLK	C3	O	SPI clock
SPI_CSB	E1	O	SPI chip select
SPI_MISO	D3	I	SPI main in, subnode out
SPI_MOSI	E2	O	SPI main out, subnode in

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Table 20. SYN20708 FCBGA signal descriptions (continued)

Signal Name	Pin (Bump)	Type	Description
Supplies			
BT_VDD_MISCLDO	L8	PWR	0.856V input supply pin for radio
BT_VDD1P8	M13	PWR	1.8V input supply pin for radio
BT_VDD3P3_CORE0	J11	PWR	3.3V input supply pin for radio
BT_VDD3P3_CORE1	E11	PWR	3.3V input supply pin for radio
OTP_VDD1P8	N6	PWR	1.8V input supply pin for OTP
VDDC	G6, H5	PWR	0.72V input supply pin for digital core logic
VDDO	E7	PWR	3.3V input supply pin for digital padring
XTAL_VDD0P9	N9	PWR	Internal power supply for radio XTAL. Requires a 1 µF off-chip capacitor for stability.
XTAL_VDD1P05	N12	PWR	1.05V input supply pin for radio XTAL oscillator circuit
Integrated Voltage Regulators			
BT_LDO_VDD1P05	G9	I	1.05V input supply pin
LDO_VDD1P05	N2	I	1.05V input supply pin
PMU_VDDIO	N4	I	VDDIO input supply pin
PMU_VDD1P8	N5	I	1.8V VDDIO input supply pin
VDDOUT_CLDO	K4	O	Nominal 0.72V digital core supply from the PMU
VDDOUT_MISCLDO	L4	O	Nominal 0.856V supply from the PMU
UART Interface			
UART_CTS	H1	I	UART clear-to-send.
UART_RTS	H2	O	UART request-to-send.
UART_RXD	G2	I	UART serial input.
UART_TXD	F2	O	UART serial output.

8.3.GPIO Signals and Strapping Options

The pins listed in Table 21 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 21 provides the SYN20708 GPIO strapping options.

Table 21. SYN20708 GPIO strapping options

Pin Name	Default Pull During Strapping[a]	Description
ANT_SEL3	0	GPIO configuration during test mode (TEST_ENABLE = 1): 0: Shared GPIOs are used as needed. 1: All GPIOs are configured as inputs. Typically not used for the SYN20708.

a. The default pull-up and pull-down conditions indicated in this table apply only during strap sampling, which occurs shortly after an internal POR or deassertion of an external POR. For VDDIO, the pull-up and pull-down ranges are 35–65 kΩ (50 kΩ, typical).

8.4.GPIO Alternative Signal Functions

Table 22. Core-level Mux selection

Pin	Function Number											
	0	1	3	4	5	6	7	11	12	13	14	15
BT_UART_CTS_N	UART_CTS_N	—	—	—	UART2_RTS_N	—	A_GPIO[1]	—	—	SPI_CSB	—	—
BT_UART_RTS_N	UART_RTS_N	—	—	—	UART2_CTS_N	—	A_GPIO[0]	—	—	SPI_MISO	—	—
BT_UART_RXD	UART_RXD	—	—	SDA	UART2_RXD	—	GPIO[5]	—	—	SPI_MOSI	—	—
BT_UART_TXD	UART_TXD	—	—	SCL	UART2_TXD	—	GPIO[4]	—	—	SPI_CLK	—	—

Table 22. Core-level Mux selection

Pin	Function Number											
	0	1	3	4	5	6	7	11	12	13	14	15
BT_CORE_SIG_0	A_GPIO[0]	—	—	—	—	—	—	—	—	—	—	SPI_CLK
BT_CORE_SIG_1	A_GPIO[1]	—	—	—	—	—	—	—	—	—	—	SPI_CSB
BT_CORE_SIG_2	A_GPIO[2]	—	—	—	—	—	—	—	SDA	—	—	SPI_MOSI
BT_CORE_SIG_3	A_GPIO[3]	—	—	—	—	—	—	—	SCL	—	—	SPI_MISO
BT_CORE_SIG_4	A_GPIO[5]	—	—	—	—	—	—	UART2_RTS_N	SCL	—	—	SPI_MOSI
BT_CORE_SIG_5	A_GPIO[6]	—	—	—	—	—	—	UART2_CTS_N	—	SDA	—	SPI_MISO
BT_CORE_SIG_6	GPIO[7]	—	—	—	—	—	—	UART2_RXD	—	—	—	SPI_CSB
BT_CORE_SIG_7	GPIO[6]	—	—	—	—	—	—	UART2_TXD	—	—	—	SPI_CLK
BT_CORE_SIG_8	GPIO[1]	—	—	—	—	—	—	—	—	—	—	—
BT_CORE_SIG_9	—	—	—	—	—	—	A_GPIO[7]	—	—	—	—	—
BT_CORE_SIG_10	GPIO[0]	—	—	—	—	—	—	—	—	—	—	—
BT_GPIO5	GPIO[5]	—	—	—	—	—	—	UART2_CTS_N	—	—	—	SCL
BT_GPIO4	GPIO[4]	—	—	—	—	—	—	UART2_RTS_N	—	—	—	SDA
BT_GPIO3	GPIO[3]	UART2_TXD	—	—	—	—	—	—	—	—	—	—

Table 22. Core-level Mux selection

Pin	Function Number											
	0	1	3	4	5	6	7	11	12	13	14	15
BT_GPIO2	GPIO[2]	—	UART2_RTS_N	—	—	—	—	—	—	—	—	—
BT_AJTAG_TDI	AJTAG_TDI	—	—	SPI_MISO	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	SDA
BT_AJTAG_TDO	AJTAG_TDO	—	—	SPI_MOSI	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	SCL
BT_AJTAG_TMS	AJTAG_TMS	—	—	SPI_CSB	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	—
BT_AJTAG_TCK	AJTAG_TCK	—	—	SPI_CLK	GPIO[5]	GPIO[6]	GPIO[7]	—	A_GPIO[4]	A_GPIO[5]	A_GPIO[6]	—

Table 23. Top-level Mux selection

Pad Name	Function Number			
	0 (Default)	1	2	3
TDI	BT_AJTAG_TDI	BT_AJTAG_TDI	BT_AJTAG_TDI	BT_AJTAG_TDI
TDO	BT_AJTAG_TDO	BT_AJTAG_TDO	BT_AJTAG_TDO	BT_AJTAG_TDO
TMS	BT_AJTAG_TMS	BT_AJTAG_TMS	BT_AJTAG_TMS	BT_AJTAG_TMS
TCK	BT_AJTAG_TCK	BT_AJTAG_TCK	BT_AJTAG_TCK	BT_AJTAG_TCK
UART_CTS	BT_UART_CTS_N	BT_UART_CTS_N	BT_UART_CTS_N	BT_UART_CTS_N
UART_RTS	BT_UART_RTS_N	BT_UART_RTS_N	BT_UART_RTS_N	BT_UART_RTS_N
UART_RXD	BT_UART_RXD	BT_UART_RXD	BT_UART_RXD	BT_UART_RXD
UART_TXD	BT_UART_TXD	BT_UART_TXD	BT_UART_TXD	BT_UART_TXD
SPI_CLK	BT_CORE_SIG_0	BT_CORE_SIG_0	BT_CORE_SIG_0	BT_CORE_SIG_0
SPI_CSB	BT_CORE_SIG_1	BT_CORE_SIG_1	BT_CORE_SIG_1	BT_CORE_SIG_1
SPI_MISO	BT_CORE_SIG_2	BT_CORE_SIG_2	BT_CORE_SIG_2	BT_CORE_SIG_2
SPI_MOSI	BT_CORE_SIG_3	BT_CORE_SIG_3	BT_CORE_SIG_3	BT_CORE_SIG_3
SECI_IN	SECI_IN	—	TX_CONFX	—
SECI_OUT	SECI_OUT	—	RF_ACTIVE	—
BT_STATUS	BT_CORE_SIG_9	—	—	BT_STATUS
TX_CONFX2	BT_CORE_SIG_6	—	—	TX_CONFX2
RF_ACTIVE2	BT_CORE_SIG_8	—	—	RF_ACTIVE2
BT_STATUS2	BT_CORE_SIG_7	—	—	BT_STATUS2
ANT_SEL0	ANT_SEL0	BT_CORE_SIG_10	—	—
ANT_SEL1	ANT_SEL1	BT_CORE_SIG_4	BT_CORE_SIG_7	ANT_SEL1
ANT_SEL2	ANT_SEL2	BT_CORE_SIG_5	BT_CORE_SIG_6	ANT_SEL2
ANT_SEL3	ANT_SEL3	BT_GPIO3	—	—
EPA_CTRL0	EPA_CTRL0	BT_GPIO4	—	—
EPA_CTRL1	EPA_CTRL1	BT_GPIO5	—	—
ETRSW_CTRL0	ETRSW_CTRL0	BT_CORE_SIG_6	—	—
ETRSW_CTRL1	ETRSW_CTRL1	BT_CORE_SIG_7	—	—

8.5.I/O States

The following notations are used in Table 24:

- I: Input signal
- O: Output signal
- Hold: Last value on input is held
- I/O: Input/Output signal
- PU: Pulled up
- PD: Pulled down
- No Pull: Neither pulled up nor pulled down

Table 24. Bluetooth system I/O states

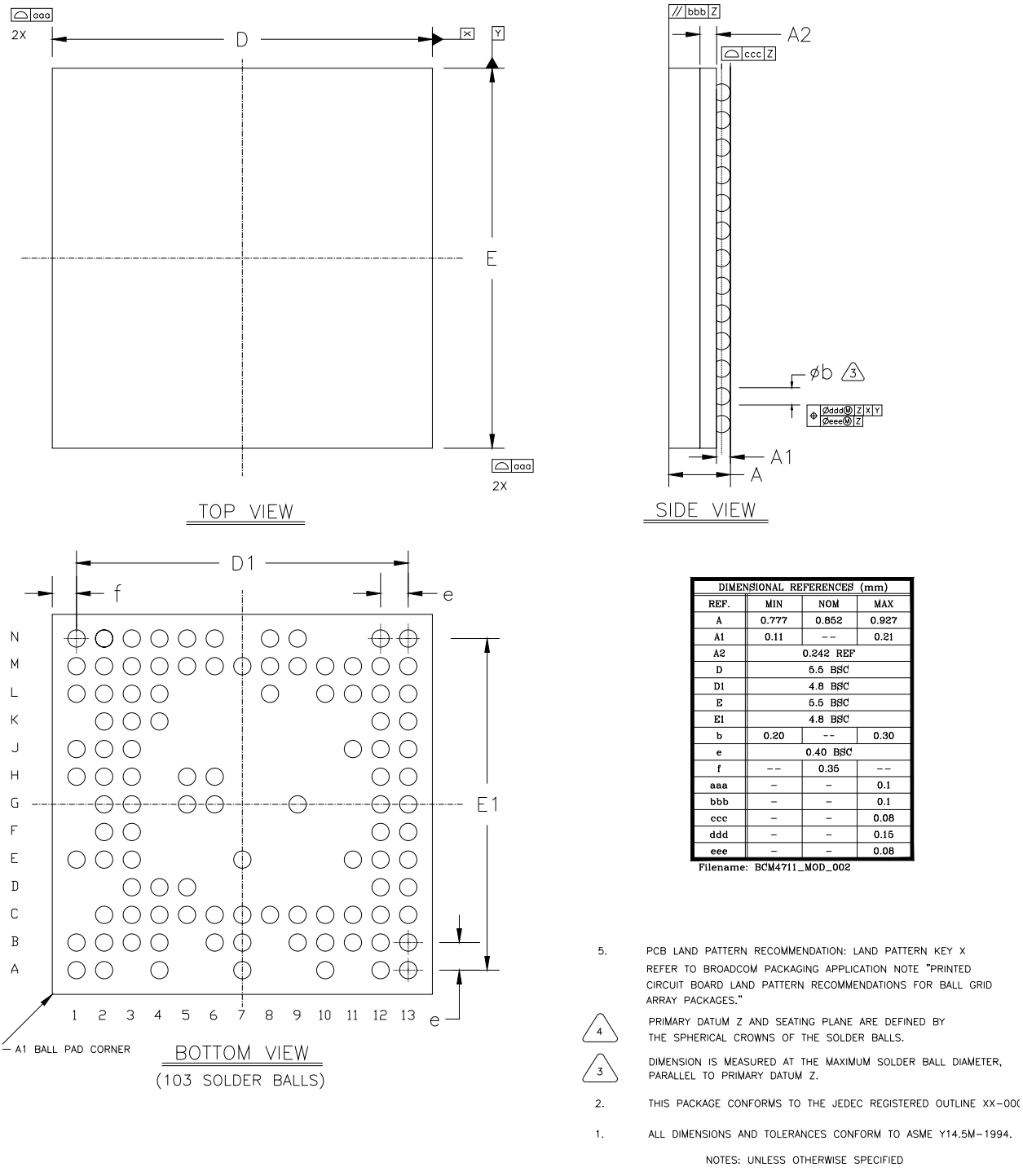
Name	Keeper	Power Applied (BT_REG_ON = 1) and VDDIOs Present; BT Subsystem Is in Reset	Out-of-Reset; Before FW Boot
BT_REG_ON	N	I, PD (of 100 kΩ)	I, PD (of 100 kΩ)
ANT_SEL0	Y	I, No Pull, input disable	I, PD
ANT_SEL1	Y	I, No Pull, input disable	I, PD
ANT_SEL2	Y	I, No Pull, input disable	I, PD
ANT_SEL3	Y	I, No Pull, input disable	I, No Pull
BT_STATUS	Y	I, No Pull, input disable	I, PD
BT_STATUS2	Y	I, No Pull, input disable	I, PD
BT_UART_CTS	Y	I, No Pull, input disable	I, PU
BT_UART_RTS	Y	I, No Pull, input disable	I, PU
BT_UART_RXD	Y	I, No Pull, input disable	I, PU
BT_UART_TXD	Y	I, No Pull, input disable	I, PU
EPA_CTRL0	Y	I, No Pull, input disable	I, PU
EPA_CTRL1	Y	I, No Pull, input disable	I, PU
ETRSW_CTRL0	Y	I, No Pull, input disable	I, PD
ETRSW_CTRL1	Y	I, No Pull, input disable	I, PD
HW_RESET_B	Y	I, PU	I, PU
MODE_SEL	Y	I, No Pull	I, No Pull
RF_ACTIVE2	Y	I, No Pull, input disable	I, No Pull
SECI_IN	Y	I, No Pull, input disable	I, PD
SECI_OUT	Y	I, No Pull, input disable	I, PD
SPI_CLK	Y	I, No Pull, input disable	I, PD
SPI_CSB	Y	I, No Pull, input disable	I, PU
SPI_MISO	Y	I, No Pull, input disable	I, PD
SPI_MOSI	Y	I, No Pull, input disable	I, PD
SW_RESET_B	Y	I, PU	I, PU

Table 24. Bluetooth system I/O states (continued)

Name	Keeper	Power Applied (BT_REG_ON = 1) and VDDIOs Present; BT Subsystem Is in Reset	Out-of-Reset; Before FW Boot
SYS_RESET_B	Y	I, PU	I, PU
TEST_ENABLE	Y	I, PD	I, PD
TX_CONFX2	Y	I, No Pull, input disable	I, PD

8.6.Package Drawing

Figure 15 is a mechanical outline drawing (MOD) for the SYN20708 FCBGA.



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.777	0.852	0.927
A1	0.11	--	0.21
A2	0.242 REF		
D	5.5 BSC		
D1	4.8 BSC		
E	5.5 BSC		
E1	4.8 BSC		
b	0.20	--	0.30
e	0.40 BSC		
f	--	0.35	--
aaa	–	–	0.1
bbb	–	–	0.1
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: BCM4711_MOD_002

5. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY X REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

4 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE XX-00(

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 15. SYN20708 FCBGA mechanical outline drawing

8.7.Package Thermal Characteristics

Table 25. SYN20708 package thermal characteristics

Characteristic	Value
θ_{JA} (°C/W) (value in still air)	32.11
θ_{JB} (°C/W)	13.33
θ_{JC} (°C/W)	21.61
Ψ_{JT} (°C/W)	3.99
Ψ_{JB} (°C/W)	13.38
Maximum Junction Temperature T_j (°C)	98.8

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9.Ordering Information

Table 26. Ordering information

Part Number	Package	Description	Ambient Operating Temperature
Pre-Production Ordering			
SYN20708A0IFFBG	5.5 mm × 5.5 mm, 103-pin FCBGA	2.4 GHz, 2x2 (or 1+1) dual-radio Bluetooth 5.4 and IEEE 802.15.4	–40°C to 85°C

10.Revision History

Revision	Description
1	Initial Synaptics Release
2	Updated Ordering Information table
3	Updated RF specification

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