Application Note

SL1620 General PCB Design and DDR4 & DDR3 Interface Layout Guidelines

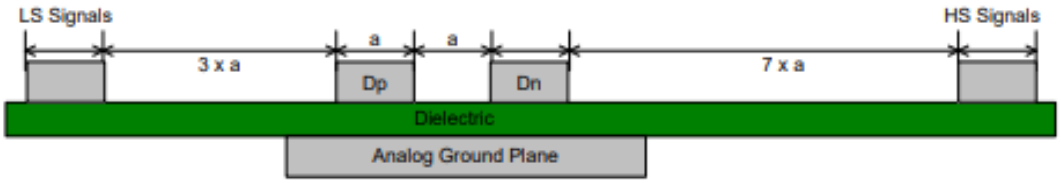
Abstract: This document provides PCB design and layout guidelines for integrating the Synaptics SL1620 with DDR4 and DDR3 memory, detailing routing rules, power supply considerations, impedance requirements, and best practices to ensure optimal signal integrity and performance.

  | PN: 506-001393-01 Rev F

Contents

1. PCB Layout Guidelines

- Trace impedance of 100ohm differential (+/-10%) is required. For USB2.0, the trace impedance of 90ohm differential (+/-10%) is required.
- Matching to < 0.5mm (about 0.02 inch) between two different signals. Trace lengths should match by 0.25mm (about 0.01 inch) or less for differential pairs (same pair) of high-speed signals.
- The skew between any data lane and clock lane should be matched within +/-10ps on both package and PCB.
- Do not route trace over plane void or anti-pads. Return path should be VSS and continuous.
- Ensure ground return vias adjacent to the differential pair core vias to minimize crosstalk between lanes.
- Void the planes above the BGA pads to minimize the capacitive discontinuity.
- To minimize crosstalk, take care of signal traces which are routed close to the data differential pairs. The minimum recommended spacing is 3xa for low-speed non-periodic signals and 7xa for high-speed periodic signals. A continuous ground plane below the differential lines is required.



- TX and RX pairs should not be routed side-by-side in the same signal layer.
- Crosstalk should be accumulated total with all aggressors and meet the
- -30dB requirement until Nyquist frequency.
- The insertion loss of the trace is < 3dB (at Nyquist). For PCIE3.0, USB3.0 and Ethernet, the insertion loss of trace can be < 6dB. It should be monotonic, with no large insertion loss variations (+/-2dB) in the Nyquist frequency range. Trace should be shortest and low-loss as possible.

2. Power Supply Guidelines

- Supply bypass capacitors are recommended to minimize power supply noise. Noise analysis of the power delivery network is required to determine the actual values. Depending on their size, each capacitor will have a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that will determine the given capacitor's effectiveness over a frequency range. In general, several low-value capacitors (ceramic-type capacitors) should be placed as close as possible to the package pins. Larger-value capacitors (tantalum/electrolytic-type capacitors) can be placed farther away.
- The supply bypass capacitors should be connected as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane and trace as possible to reduce inductive and resistive losses. Typical capacitor placement can be under the package (other side of the board) or on the same side but close. An example of bypass capacitors is shown below.

Component	Value[1]
Power Supply Bypass Capacitors	0.01 µF, 0.1 µF, 4.7 µF, 10.0 µF

1. Smaller-value capacitors must be placed between the ferrite bead and the package.

- Both power plane and ground plane should be maintained continuously and have solid return path (not in bits and pieces). Pay attention to the void areas caused by vias. If the planes are cut down by vias, we need to compensate for the loss of the plane shape to make sure the effective width of the plane.

3. 4L non-HDI PCB Design Rules

3.1. NSMD Pad

- Minimum pin pitch = 0.4 mm (15.75 mil)
- Footprint pad / Paste mask of pad = 10mil (bga10)
- Solder mask of pad = 10 mil

3.2. SMD Pad

- Minimum pin pitch = 0.381 mm (15 mil)
- Footprint pad / Paste mask of pad = 12 mil (bga12)
- Solder mask of pad = 8 mil

3.3. Via

- Minimum through hole pad / Drill size = 14 / 8 mil

3.4. Spacing

- Minimum trace-to-trace = 3 mil
- Minimum trace-to-via = 3 mil
- Minimum trace-to-pad = 3 mil

The example stack-up/trace width and spacing of 4L non-HDI PCB is shown below.

Stack-up		Thickness(mil)			DK	Df	Material
	SM_TOP (0.5_PT_1OZ)	0.5			3.4		
L1			1.654	0.333oz +Plating			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L2			1.26	1oz			
	Core+PP (1.3mm)	51.18			4.6	0.018	S1000-2M
L3			1.26	1oz			
	PP (1080/RC=69%) / 0.076mm	2.99			4.14	0.019	S1000-2M
L4			1.654	0.333oz +Plating			
	SM_BOT (0.5_PT_1OZ)	0.5			3.4		
Thickness(mil):	63.988	63.988					
FinishPCBThinckness(mm):	1.6 (+/-0.16) mm						
PressPCBThinkness(mm):	1.48 (+/-0.08) mm						

Number	Type	Control Layer	Referance Layer	Adjust Line Width (mil)	Adjust Spacing (mil)	Adjust Line To Copper (mil)	Design Impedance (ohm)
1	Single-End	L1/L4	L2/L3	3.6			55.01
2	Single-End	L1/L4	L2/L3	4			52.93
3	Single-End	L1/L4	L2/L3	4.5			50.15
4	Differential	L1/L4	L2/L3	3.5	3		84.62
5	Differential	L1/L4	L2/L3	3.6	4		90.11
6	Differential	L1/L4	L2/L3	3.4	5.8		99.3
7	Differential	L1/L4	L2/L3	4	4		88.41

4. PCB Routing Rules for SL1620 DDR4/DDR3 Interface

Notes:

- This guideline recommends optimal layout practices for the DRAM section and is not a set of strict limitations.
- Synaptics reference layouts follow the guidelines, ensuring good operating timing margins.
- It is strongly recommended to copy DDR routing from the reference design.

4.1. General Rules

The general rules of usage are:

- All signals must be routed with a solid reference layer.
- Ground reference routing for all signals is preferred.
- No signal can be routed through discontinued reference.
- The impedance of single-ended signals should be targeted within a range of 50 ohms to 55 ohms, with a tolerance of +/- 10%.
- All differential signals should have a differential impedance of 85 ohms with a tolerance of +/-10%.
- Include via delay in length matching calculations.
- No more than two vias are recommended on any signal between SoC and DRAMs, excluding low speed DDR RSTn.

4.2. Placement

- The DDR4 signal pin assignments of the SL1620 are designed to allow the DDR4 chip to be placed next to SoC on top layer.
- Underneath the SoC, the decoupling capacitors for VDDM should include a combination of various capacitors that provide lower impedance from DC to 300MHz. It is highly recommended to follow the placement and values specified in the Synaptics Reference Design Kits.
- The RC components connecting to the SL1620 M0_VREF should be placed as close to the pin as possible.
- A 1% 240 ohm resister (pulldown to GND) connecting to M0_CAL should be placed as close to the pin as possible.
- The RC components connecting to SDRAM_CK0+/- should be placed as close to the SDRAM pins as possible.
- A small capacitor (2.2pF) on SDRAM_CK0+/- needs to be placed near the first DRAM (the one closest to the SoC).
- A couple of 1nF and 10nF capacitors should be placed as close as possible to each individual power pin of the SoC and all DRAMs for decoupling purpose.
- A couple of 1nF and 10nF capacitors should be placed at the edge of the power plane to reduce resonance.
- Place 1uF/10uF capacitors at the power rail input for both SoC and DRAM, to avoid power trace bottlenecking.

4.3. Routing

- The trace length difference of the DDR4/DDR3 signals (within each own group) should be maintained as follows:
  - **DQ-to-DQ (including DQS) for each Byte group:** Keep the shortest possible for each trace; trace length matching is not necessary.
  - **Address / Command (ADCM) -to-ADCM (including CLK):** Keep the shortest possible for each trace; trace length matching is not necessary.
  - **Intra-pair of Differential signals (DQS+/-, CLK+/-):** Maintain a trace length difference within 15 mils.
- The stub length from the via of each CK0+/- trace to the resistor pad should be minimized as much as the board topology, stack-up and placement constraints allow. While the general guideline is to not exceed 300 mils, in many cases the trace can be as short as 50 mils.

4.4. Package Trace Length Compensation

The following are considerations for compensation:

- Trace lengths between chip die and package pins were not matched well due to package geometry, resulting in different propagation delays for each signal on the package substrate. These differences will impact timing margin.
- When matching the trace length for each Byte group, pin delay should be accounted for.

Byte Lane 0 Group				
Pin	**Signal Net**	**DDR4 Signal**	**DDR3 Signal**	**Equivalent PCB Trace Length Based on Propagation delay Entered (mil)**
P2	M0_DQSP[0]	M0_DDR4_DQS0p	M0_DDR3_DQS0p	190.33
N2	M0_DQSn[0]	M0_DDR4_DQS0n	M0_DDR3_DQS0n	195.54
V2	M0_DM[0]	M0_DDR4_DM0	M0_DDR3_DM0	197.23
T6	M0_DQ[0]	M0_DDR4_DQ0	M0_DDR3_DQ2	125.18
T1	M0_DQ[1]	M0_DDR4_DQ1	M0_DDR3_DQ3	194.06
U3	M0_DQ[2]	M0_DDR4_DQ2	M0_DDR3_DQ0	162.14
T2	M0_DQ[3]	M0_DDR4_DQ3	M0_DDR3_DQ5	172.39
P4	M0_DQ[4]	M0_DDR4_DQ4	M0_DDR3_DQ6	151.78
U2	M0_DQ[5]	M0_DDR4_DQ5	M0_DDR3_DQ1	168.93
P6	M0_DQ[6]	M0_DDR4_DQ6	M0_DDR3_DQ4	118.64
R2	M0_DQ[7]	M0_DDR4_DQ7	M0_DDR3_DQ7	175.45

Byte Lane 1 Group				
Pin	**Signal Net**	**DDR4 Signal**	**DDR3 Signal**	**Equivalent PCB Trace Length Based on Propagation delay Entered (mil)**
W1	M0_DQSp[1]	M0_DDR4_DQS1p	M0_DDR3_DQS1p	206.70
W2	M0_DQSn[1]	M0_DDR4_DQS1n	M0_DDR3_DQS1n	201.21
W6	M0_DM[1]	M0_DDR4_DM1	M0_DDR3_DM1	123.28
U6	M0_DQ[8]	M0_DDR4_DQ8	M0_DDR3_DQ13	126.55
AA1	M0_DQ[9]	M0_DDR4_DQ9	M0_DDR3_DQ8	209.73
W7	M0_DQ[10]	M0_DDR4_DQ10	M0_DDR3_DQ11	105.79
Y2	M0_DQ[11]	M0_DDR4_DQ11	M0_DDR3_DQ12	189.13
W3	M0_DQ[12]	M0_DDR4_DQ12	M0_DDR3_DQ15	173.81
AA2	M0_DQ[13]	M0_DDR4_DQ13	M0_DDR3_DQ14	195.80
W4	M0_DQ[14]	M0_DDR4_DQ14	M0_DDR3_DQ9	141.00
AB2	M0_DQ[15]	M0_DDR4_DQ15	M0_DDR3_DQ10	183.74
Byte Lane 2 Group				
Pin	**Signal Net**	**DDR4 Signal**	**DDR3 Signal**	**Equivalent PCB Trace Length Based on Propagation delay Entered (mil)**
AC2	M0_DQSp[2]	M0_DDR4_DQS2p	M0_DDR3_DQS2p	214.38
AC1	M0_DQSn[2]	M0_DDR4_DQS2n	M0_DDR3_DQS2n	217.80
AF2	M0_DM[2]	M0_DDR4_DM2	M0_DDR3_DM2	218.32
AE4	M0_DQ[16]	M0_DDR4_DQ16	M0_DDR3_DQ18	171.01
AF1	M0_DQ[17]	M0_DDR4_DQ17	M0_DDR3_DQ19	226.97
AC6	M0_DQ[18]	M0_DDR4_DQ18	M0_DDR3_DQ16	158.43
AD3	M0_DQ[19]	M0_DDR4_DQ19	M0_DDR3_DQ21	188.75
AC4	M0_DQ[20]	M0_DDR4_DQ20	M0_DDR3_DQ22	182.60
AE3	M0_DQ[21]	M0_DDR4_DQ21	M0_DDR3_DQ17	202.93
AC7	M0_DQ[22]	M0_DDR4_DQ22	M0_DDR3_DQ20	156.91
AD2	M0_DQ[23]	M0_DDR4_DQ23	M0_DDR3_DQ23	211.67

Byte Lane 3 Group				
Pin	Signal Net	DDR4 Signal	DDR3 Signal	Equivalent PCB Trace Length Based on Propagation delay Entered (mil)
AH1	M0_DQSp[3]	M0_DDR4_DQS3p	M0_DDR3_DQS3p	245.19
AJ1	M0_DQSn[3]	M0_DDR4_DQS3n	M0_DDR3_DQS3n	242.23
AK2	M0_DM[3]	M0_DDR4_DM3	M0_DDR3_DM3	238.19
AH2	M0_DQ[24]	M0_DDR4_DQ24	M0_DDR3_DQ27	216.37
AL3	M0_DQ[25]	M0_DDR4_DQ25	M0_DDR3_DQ24	237.31
AE6	M0_DQ[26]	M0_DDR4_DQ26	M0_DDR3_DQ31	165.81
AJ2	M0_DQ[27]	M0_DDR4_DQ27	M0_DDR3_DQ28	225.48
AG4	M0_DQ[28]	M0_DDR4_DQ28	M0_DDR3_DQ29	196.17
AL4	M0_DQ[29]	M0_DDR4_DQ29	M0_DDR3_DQ30	216.70
AJ3	M0_DQ[30]	M0_DDR4_DQ30	M0_DDR3_DQ25	203.98
AM4	M0_DQ[31]	M0_DDR4_DQ31	M0_DDR3_DQ26	227.84

ADDRESS / COMMAND / CONTROL Group				
Pin	Signal Net	DDR4 Signal	DDR3 Signal	Equivalent PCB Trace Length Based on Propagation delay Entered (mil)
M3	M0_CKp	M0_DDR4_CKp	M0_DDR3_CKp	179.68
M4	M0_CKn	M0_DDR4_CKn	M0_DDR3_CKn	180.65
C4	M0_A[0]	M0_DDR4_A0	M0_DDR3_A11	198.08
H6	M0_A[1]	M0_DDR4_A1	M0_DDR3_A2	165.55
K6	M0_A[2]	M0_DDR4_A2	M0_DDR3_A6	149.73
J3	M0_A[3]	M0_DDR4_A3	M0_DDR3_A15	181.94
H2	M0_A[4]	M0_DDR4_A4	M0_DDR3_A0	228.18
G2	M0_A[5]	M0_DDR4_A5	M0_DDR3_A12	197.44
F3	M0_A[6]	M0_DDR4_A6	M0_DDR3_A5	209.42
F2	M0_A[7]	M0_DDR4_A7	M0_DDR3_A4	225.36
F4	M0_A[8]	M0_DDR4_A8	M0_DDR3_A9	204.51
C1	M0_A[9]	M0_DDR4_A9	M0_DDR3_A7	248.83
K7	M0_A[10]	M0_DDR4_A10	M0_DDR3_A3	131.16
B4	M0_A[11]	M0_DDR4_A11	M0_DDR3_A8	225.23
K3	M0_A[12]	M0_DDR4_A12	M0_DDR3_A10	190.45
H3	M0_A[13]	M0_DDR4_A13	M0_DDR3_A1	194.53
D3	M0_ACTn	M0_DDR4_ACTn	M0_DDR3_A13	244.12
C3	M0_BA[0]	M0_DDR4_BA0	M0_DDR3_BA0	230.86
D2	M0_BA[1]	M0_DDR4_BA1	M0_DDR3_BA1	227.76
C2	M0_BG	M0_DDR4_BG0	M0_DDR3_BA2	253.59
H1	M0_CASn	M0_DDR4_CASn	M0_DDR3_CASn	226.71
J2	M0_CKE	M0_DDR4_CKE	M0_DDR3_CKE	212.16
M2	M0_CSn	M0_DDR4_CSn	M0_DDR3_CSn	212.96
L2	M0_ODT	M0_DDR4_ODT	M0_DDR3_ODT	215.68
L1	M0_RASn	M0_DDR4_RASn	M0_DDR3_RASn	207.24
A5	M0_RSTn	M0_DDR4_RSTn	M0_DDR3_RSTn	227.17
F1	M0_WEn	M0_DDR4_Wen	M0_DDR3_WEn	238.27
B5	M0_NC	M0_DDR4_NC	M0_DDR3_A14	221.50
M7	M0_CAL	M0_DDR4_CAL	M0_DDR3_CAL	114.90

4.5. Layer PCB Routing Example: Recommended Design Rules

1. **Footprint**

   Please follow the dimension drawing in the Synaptics Datasheet. Pay attention to the size of the pad and solder mask opening.

   - **Pad size:** 10 mil
   - **Solder mask opening size**: 10 mil

2. **Layout Design Rule**

   - **PCB board thickness:** 1.6mm
   - **4-layer PCB**
   - **Single-ended trace width:** 4 mil
   - **Single-ended trace impedance:** 55+/-10% ohms
   - **Differential-pair trace width/spacing**: 4.5/4 mil
   - **Differential-pair trace impedance:** 85+/-10% ohms
   - **Minimum via (mechanical drilling) size:** 8 mil
   - **Maximal annulus of via:** 16 mil
   - **Minimum spacing (excluding BGA area):**
     - **Pad to pad:** 4 mil
     - **Pad to trace:** 4 mil
     - **Pad to via:** 4 mil
     - **Trace to trace:** 4 mil
     - **Trace to via:** 4 mil
     - **Via to via:** 4 mil

3. **PCB stack-up**

Layer Name	Thickness	Dk @ 1GHz
Top SM	1.18 mil	3.8
Cu1	0.333oz + Planting	
Dielectric	3.2 mil	4.5
Cu2	1 oz	
Core	48.38	4.5
Cu3	1 oz	
Dielectric	3.2 mil	4.5
Cu4	0.333oz + Planting	
Bottom SM	1.18 mil	3.8

4.5.1. Placement and Routing Recommendations

This placement and routing of Synaptics reference design were based on intensive signal integrity (SI) simulations, including model extraction and transient analyst, to ensure timing closure. This is particularly sensitive for 4-layer PCBs due to the non-homogeneous nature of the micro-strip line.

Single set of fixed routing rules: It is not possible to provide one single set of fixed detailed routing rules for all designs.

Recommendation: Follow the PCB layout of Synaptics reference design.

Custom PCB layout: If a custom PCB layout is used, it is crucial to close timing with proper SI simulation to ensure proper functionality.

5. Revision History

Revision	Description
A	Initial release.
B	Release as Public document.
C	Updated Routing section.
D	Added the following sections: • 1 PCB Layout Guidelines • 2 Power Supply Guidelines • 3 4L non-HDI PCB Design Rules
E	Minor update to document title.
F	Minor update to latest template.

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