Application Note

Astra™ Machina Foundation Series SPI

Abstract: This application note provides detailed connection and guidelines of the Serial Peripheral Interface (SPI) with the SL1620, SL1640 and SL1680 RDK.

  | PN: 506-001608-01 Rev A

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1. Overview

The Serial Peripheral Interface (SPI) is a high-speed, full-duplex communication protocol widely used for interfacing microcontrollers, SoCs, and peripheral devices such as sensors, EEPROMs, ADCs, DACs, and display controllers. Astra RDK provides a built-in SPI controller that supports various modes, clock speeds, and multiple target devices (maximum four devices).

This application note focuses on the hardware design considerations for implementing SPI in Astra RDK-based designs, including SPI Boot mode.

The SL16x0 processor includes 2 SPI controllers. For SL1680 and SL1640, one of SPI operates on SM domain. Each SPI interface supports up to four target devices.

The primary features of **SoC SPI** controller are:

- 4 CS pins
- SPI host and target mode
- DMA mode
- Maximum SPI clock 50 MHz
- SPI mode 0, 1, 2, 3
- 1.8V I/O Voltage
- SPI Boot mode supported (with CS0 only)

The primary features of **SM SPI** controller are:

- 4 CS pins
- SPI host and target mode
- Maximum SPI clock 12.5 MHz
- SPI mode 0, 1, 2, 3
- 1.8V I/O Voltage

2. Hardware Connection of SPI1 on SL16x0 RDK

The SPI1 interface on the SL16x0 RDK is connected to an on-board SPI flash (W25Q128JWSIQ) for SPI boot. The remaining three chip select (CS) pins are pin-muxed to other functions. Additionally, a 2×6 header is provided on the I/O board to facilitate connections with an external SPI key for debugging purposes.

Figure 1 illustrates the location of the 2×6 header on the I/O board.

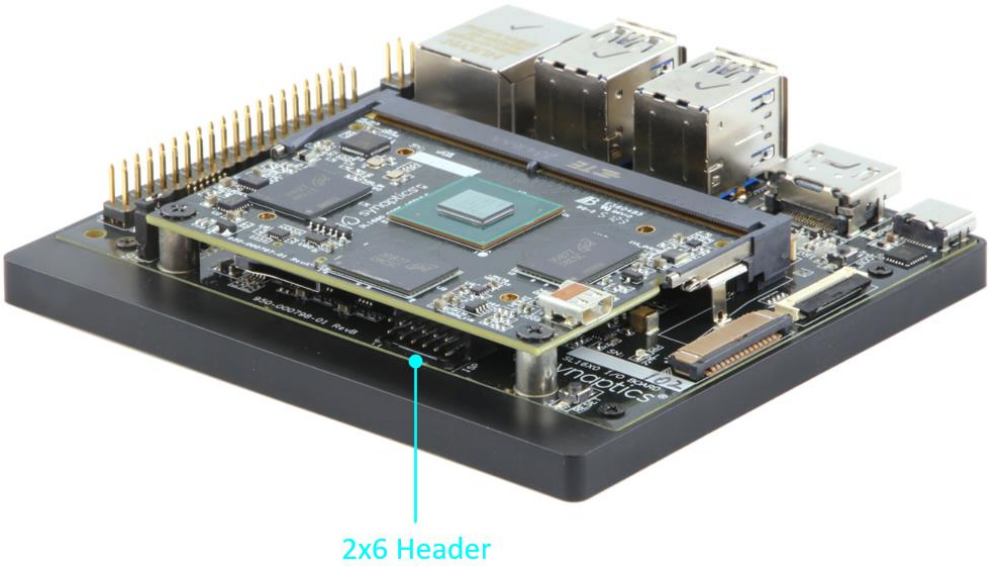

Figure 1. Overview of Astra Machina Foundation Series

2.1. Hardware Connection

Figure 2 illustrates the hardware connections of SPI1 on the SL16x0 RDK platform. The design enables seamless boot mode switching between on-board SPI Flash, external SPI key, and eMMC, ensuring flexible boot options.

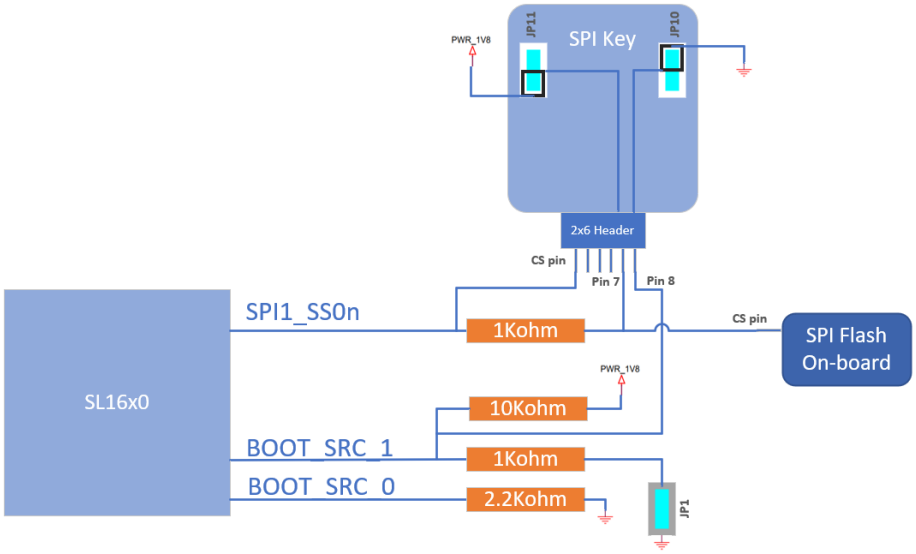

Figure 2. SPI1 connection of SL16x0 RDK

2.2. Boot mode of SL16x0 RDK

- **On-board SPI Boot—**SPI1 is connected to the on-board SPI Flash and is used as the primary boot source.
  - Leave 2x6 Header open
  - Short JP1
  - BOOT_SRC[1:0] = 2'b00
- **External SPI Key Boot—**SPI1 is connected to both the on-board SPI Flash and the external SPI key. However, the chip select (CS) pin of the on-board SPI Flash is directly tied to 1.8V, effectively bypassing it and preventing it from being selected during communication.
  - JP10 to 2-3, JP11 to 1-2
  - JP1 no effect
  - BOOT_SRC[1:0] = 2'b00
- **EMMC Boot:**
  - Leave 2x6 Header open
  - Leave JP1 open
  - BOOT_SRC[1:0] = 2'b10

3. Hardware Connection of SPI2 on SL16x0 RDK

SPI2 is routed to the 40-pin header on the I/O board, enabling SPI peripheral expansion. To enhance compatibility with external SPI devices, the I/O voltage of SPI2 on the 40-pin header is converted to 3.3V using an on-board level shifter.

Figure 3 illustrates the location of SPI2 signals on the 40-pin header. Note that SPI2_SS2n is allocated for another function on the board, leaving only three available chip select (CS) lines for SPI peripherals.

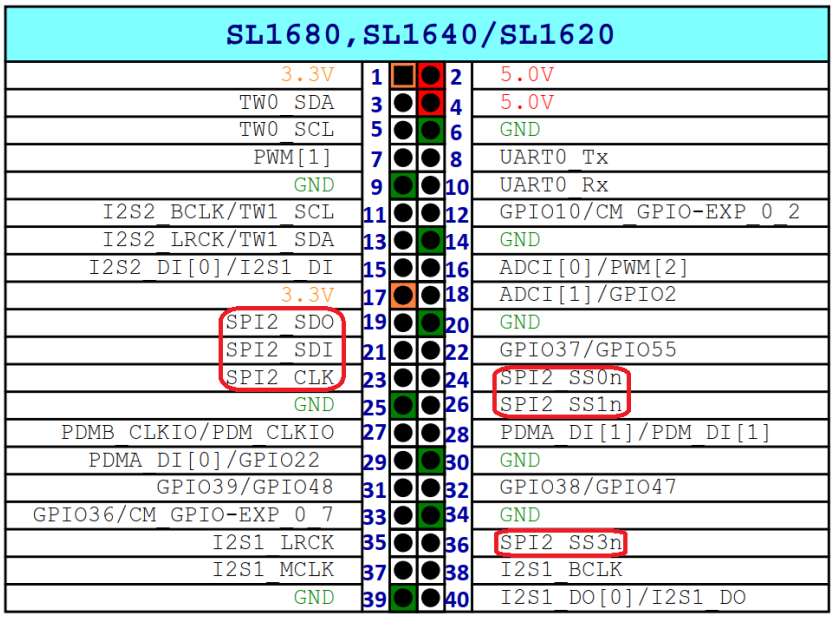

Figure 3. SPI2 pin assignment on 40 pin Header

4. Registers of SPI controller

Table 1 provides the details of the SPI Controller registers.

Table 1. SPI Controller registers

Offset	Name	Description
0x00	CTRLR0	Control Register 0 This register controls the serial data transfer.
0x04	CTRLR1	Control Register 1 This register exists only when the DW_apb_ssi is configured as a host device. Control Register 1 controls the end of serial transfers when in receive-only mode.
0x08	SSIENR	SSI Enable Register This register enables and disables the DW_apb_ssi.
0x0C	MWCR	Microwire Control Register This register controls the direction of the data word for the half-duplex Microwire serial protocol.
0x10	SER	Target Enable Register This register is valid only when the DW_apb_ssi is configured as a host device. The register enables the individual target select output lines from the DW_apb_ssi host.
0x14	BAUDR	Baud Rate Select This register is valid only when the DW_apb_ssi is configured as a host device. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value.

4.1. Base address of each SPI controller

Table 2 lists the base address of SPI on each SL16x0 processor.

Table 2. Base Address of SPI registers

SoC	TWSI Controller	Base Address
SL1680	SPI1	0xF7E81C00
	SPI2	0xF7FCA000
SL1640	**SPI1**	0xF7E81C00
	SPI2	0xF7FCA000
SL1620	**SPI1**	0xF7E82C00
	SPI2	0xF7E83000

5. References

- *Astra™ Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *SL1620 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001428-01)
- *SL1640 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001415-01)
- *SL1680 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001413-01)
- *Astra™ Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra™ Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra™ Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)

6. Revision History

Revision	Description
A	Initial release.

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